

Power Line Communications over Power Distribution  
Networks of Microprocessors – Feasibility Study,  
Channel Modeling, and a Circuit Design Approach

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# Power Line Communications over Power Distribution Networks of Microprocessors – Feasibility Study, Channel Modeling, and a Circuit Design Approach

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(ABSTRACT)

Power line communications (PLC) has been considered by utility companies for over a half century and for home networking in recent years. However, PLC at the IC level, or even at the PCB level, has not been investigated outside Dr. Ha's research group. This thesis investigates the feasibility of PLC over power distribution networks (PDNs) of advanced microprocessors. A PDN in an integrated circuit (IC) is ubiquitous as seen by the internal logic, i.e., a power line is accessible to any internal node. This suggests the possibility of monitoring or controlling the logic value of any internal node through a power line by attaching a simple sensing/control circuit to the node. Routing the data through a power line avoids the necessity of preplanning the routing of a data path between the node and an external data pin. PLC over microprocessor PDNs also provide a viable means for 'run-time testing' as well as for monitoring the so called 'large time-constant errors' resulting from aging and temperature variations.

In this thesis, we considered impulse-based ultra wideband (I-UWB) communication technology for PLC over PDNs of microprocessors. I-UWB has several advantages for PLC over PDNs due to its robustness to multipath effects, simple hardware for transmission and reception of pulses and, more importantly, reduced interference to the normal operation of microprocessors. A microprocessor PDN is heavily decoupled to damp the resonances in the power supply impedance as well as to reduce the slew rate

of current variations by locally supplying (sinking) currents to (from) the switching nodes. Consequently, a PDN behaves like a bulky lowpass filter for high frequency signals. However, the inductance component of decoupling capacitors becomes more significant beyond the self resonant frequency (SRF) of the capacitors. So, a PDN becomes essentially a distributed circuit beyond the SRF and is no longer a lowpass filter. Indeed, high frequency PDN models developed earlier at Dr. Ha's group show that there exist multiple frequency bands where high frequency signals can propagate through the PDN with relatively low attenuation [3] [4].

The major contributions of our research lie in three areas. First, we verified existence of passbands on PDN's transfer characteristics through measurements. We carried out high frequency measurements on the PDN of Intel's 65 nm Pentium processor and 45 nm Core 2 Duo processor. We measured PDN transfer characteristics up to several GHz from a core power pin on a tester board to an on-chip power node for both active and cold microprocessor dies. The measurements show the existence of narrow, sporadic and migratory passbands i.e. location of passbands change from one generation of processor to the next. The migratory nature of passbands requires the I-UWB receiver and a transmitter to cover a wide range of frequencies rather than a specific passband. Second, we have developed a PDN communication channel model for system level study. To develop the channel model, we also performed noise measurements on Intel microprocessors. The link budget was calculated based on the channel model and appropriate modulation schemes were suggested through the system level study. Third, we investigated design of an I-UWB receiver and a transmitter, which cover a wide bandwidth. The proposed receiver and transmitter designs were evaluated through simulations in TSMC 0.18  $\mu\text{m}$  CMOS process. Our simulation indicates that the PLC over a PDN is feasible with a relatively simple digital-process friendly I-UWB receiver and a transmitter.

*To my parents Thirugnanam and Alli and my sister Deepa*

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# Chapter 1: Introduction

## ***1.1 Problem and Motivation***

Testing and debug strategies have to be constantly re-invented in order to keep pace with the increasing complexity of a modern microprocessor. Currently, there exists no systematic method to diagnose a system after it crashes and fails to reboot. Also, it is difficult to continuously monitor errors that creep up over a period of time due to variations in temperature and simply aging. To support resilient operations in these constantly varying conditions, extensive monitoring is required throughout the die. Although self-test circuits are used to estimate these variations on a microprocessor die, most of the test circuits are either removed once the chip is deployed on the field or offer very limited access [1][2].

The Power Distribution Network (PDN) is ubiquitous across a microprocessor, i.e. a power line is accessible to any internal node. If the power line can be used to communicate with the external world, it can avoid preplanned routing of a data path from a node to an external data pin. This is a highly attractive feature for testing, as the routing of data paths is expensive in design time as well as in silicon area. Since the internal nodes can either be controlled or observed readily, faults in enormously large and complex ICs like microprocessors can easily be identified and characterized. Considering the time and effort spent on testing and verifying processors, this ability could possibly reduce the important ‘time to market’. Further, the ability to monitor internal node values without routing data paths opens up a possibility for fault diagnosis, monitoring transient logic values during built-in self test, sending control data to sensors and for on-line testing.

The use of power lines in an IC environment was introduced by Dr. Ha’s group in [3] and extended to massive scan-chains in [4]. As noted in [3][4], PLC in a microprocessor faces a different set of technical challenges from that of traditional PLC as described below. Most importantly, the noise characteristics of the PDN are different from a traditional PLC. Secondly, the signal power level in the PDN should be

sufficiently small not to disturb the correct operation of the circuit, which makes the recovery of data from a noisy power line difficult. Finally, a microprocessor PDN is heavily decoupled to damp the resonances in the power supply impedance as well as reduce the slew rate of current variations by locally supplying (sinking) currents to (from) the switching nodes. Consequently, the PDN looks like a bulky low pass filter for high frequency signals. However, it is well known that the inductance in the decoupling capacitors becomes significant beyond the self resonant frequency of the capacitors. Also, at microwave frequencies, the PDN is essentially a distributed circuit and as shown in [3] [4], there exists some band of frequencies where the attenuation through the PDN is low. This band of frequencies can be used for communication over the PDN.

## **1.2 System Overview and Application Scenarios**

I-UWB has several advantages for PLC over PDNs due to its robustness to multipath effects, simple hardware for transmission and reception of pulses and, more importantly, reduced interference to the normal operation of microprocessors. Communication over the power lines in a microprocessor PDN can be one-way or two-way. Using one-way communication, internal nodes can be monitored and only I-UWB receivers need to be implemented on-chip. In two-way communication, internal nodes can be monitored and/or controlled; however, in this case both I-UWB transmitters and receivers should be implemented on-chip. The two application scenarios are discussed in more detail in the following sections.

### **1.2.1 One-way communication**

One-way communication is shown in Figure 1.1 . In this scenario, the proposed communication method is used for internal node monitoring purposes. Receivers are placed at different node locations and an external chip placed on the test/mother board

is used to monitor the data. The main application would be the ability to control internal nodes or over-write register values during testing/debug. Different receivers can be identified by assigning them a specific code as in conventional wireless communication.

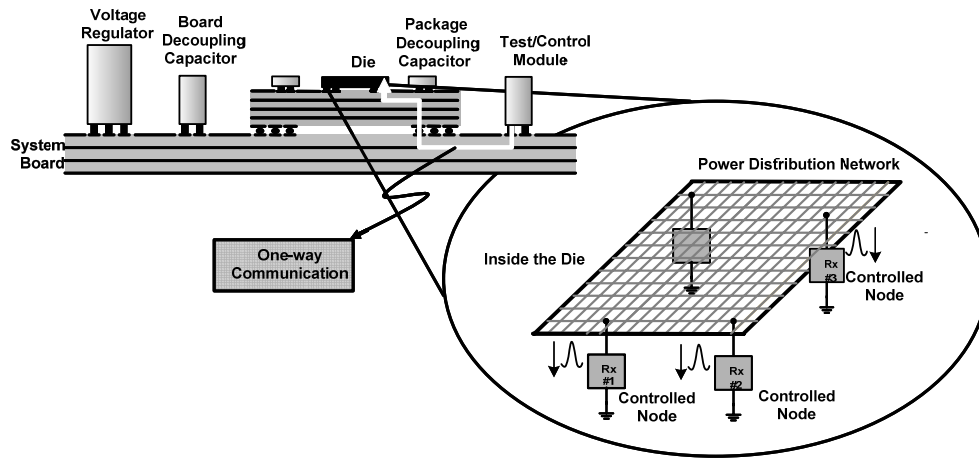


Figure 1.1: Schematic of the application scenario #1

## 1.2.2 Two-way communication

Two-way communication over the PDN is shown in Figure 1.2. The communication method can be used for both control and monitoring of internal nodes. Two-way communication requires a transmitter and receiver at each of the nodes to be monitored/controlled and will be considerably power hungry. Overdriving pulses on the PDN using an internal transmitter is highly power intensive because a large amount of current has to be drawn (or driven) in order to produce even low amplitude pulses on the PDN. Two-way communication enables the ability to monitor variations due to temperature/aging. Even though the transmitter would be power-intensive, the link need not be active continuously. The link can be activated sporadically and the variations can be monitored online or stored for later assessment.

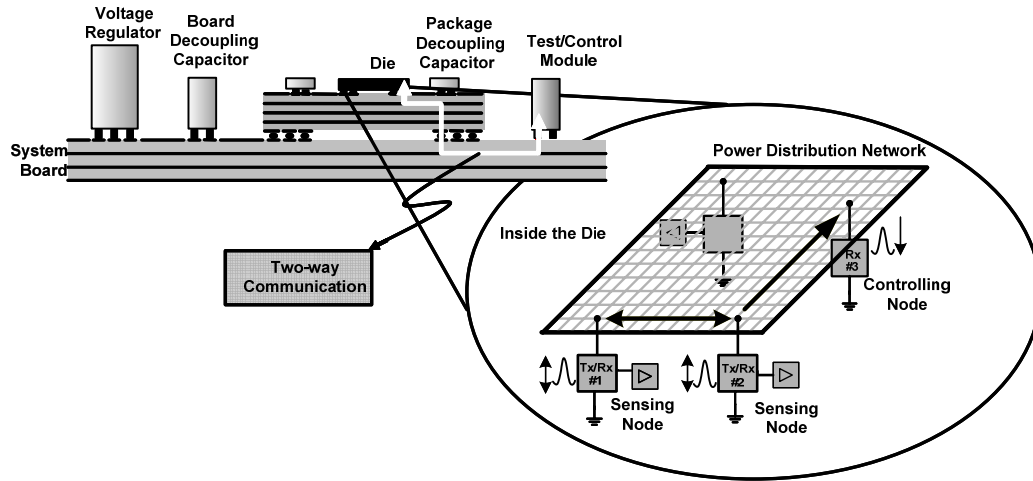


Figure 1.2: Schematic of the application scenario #2

### 1.3 The Feasibility

One of the most important questions to be answered for proceeding with the research proposal is to address the concerns regarding its feasibility. Therefore the question of feasibility is addressed briefly here and will be discussed in more detail in chapters 3 and 4.

To reduce the voltage sag resulting from PDN impedance resonances and noise resulting from the enormous switching activity, the microprocessor PDN is decoupled with capacitors on the board, package and at the chip-level. The decoupling network also filters out the high frequency noise on the power distribution network. This makes the overall power distribution network resemble a bulky low pass filter. However, a more complete model of the decoupling capacitor shown in Figure 1.3 indicates cause for optimism and possible existence of passbands in the high frequency PDN transfer characteristics. The model shown in Figure 1.3 takes into account the Effective Series Resistance (ESR) and the effective series inductance (ESL) as well as the actual capacitance.

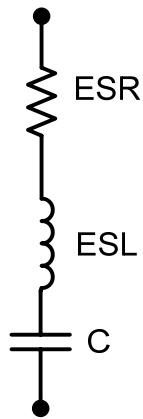


Figure 1.3: Equivalent model of the decoupling capacitor

Although the decoupling capacitors make the power distribution network resemble a bulky low pass filter, the inductance in the capacitors dominate than the SRF of the capacitors. Figure 1.4 shows the impedance vs. the frequency of the decoupling capacitors typically used in microprocessor packages. It can be observed that the impedance is capacitive (i.e. decreases with increasing frequency) at lower frequencies and beyond SRF the impedance becomes inductive (i.e. increases with increasing frequency). The SRF of all the capacitors shown in Figure 1.4 occurs in the vicinity of 100 MHz. Another observation is that the SRF of larger capacitors is lower because large capacitors have a bigger associated inductance.

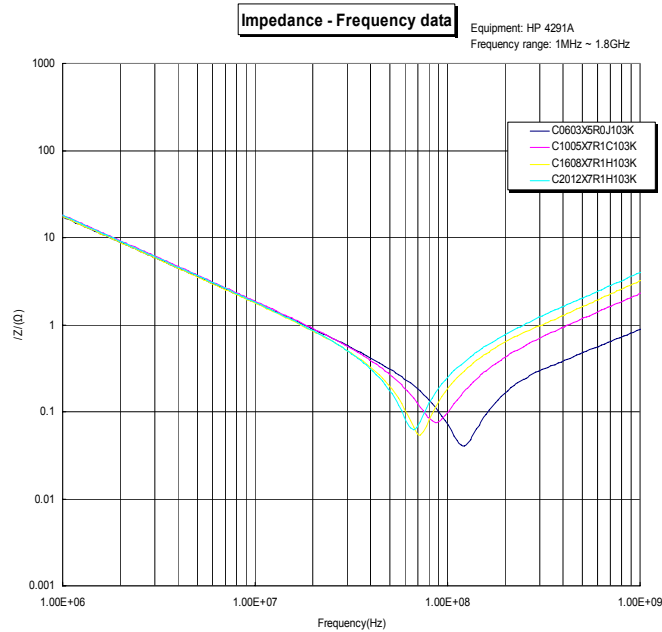


Figure 1.4: Impedance vs. frequency of decoupling capacitors in microprocessors

Further, at microwave frequencies ( $> 1$  GHz), the microprocessor package dimensions are of the order of the wavelength and the PDN essentially becomes a distributed circuit. Under the distributed circuit assumption, the order of the PDN circuit equivalent increases dramatically and complex interaction between ‘resonances’ of the different inductive and capacitive elements in the circuit equivalent leads to very different transfer characteristics than those observed from a lumped PDN equivalent model (including existence of high frequency pass bands). More details on the distributed circuit assumption and high frequency PDN modeling is provided in Chapter 3.

## 1.4 Organization and Dissertation Research Topics

The dissertation is organized as follows; Chapter 2 discusses the necessary preliminaries in regards to the research proposal. Some theoretical background and advantages of ultra wideband (UWB) signaling is presented, followed by the various

pulse modulation techniques and the more established applications of UWB technology. Next, the parallel idea, power line communications over residential power delivery networks is discussed. The power line communications, its history, signaling and noise characteristics are discussed. A review of power line modems reported in the literature is provided. Finally, the PDN design in microprocessors is described. The chapter gives insight into the design philosophy for PDN in microprocessors and concludes with the decoupling techniques for PDN impedance control and switching noise reduction.

In chapter 3, feasibility study conducted through detailed PDN modeling is described. PDN models developed previously at Dr. Ha's research group were studied. Models included the package, on-chip power grid as well as the decoupling capacitors. Feasibility was studied by simulating the PDN transfer characteristics as a function of frequency. Simulations indicated the existence of several pass bands beyond 1 GHz. To validate the models and to verify the existence of pass bands, proprietary PDN models developed at Intel microprocessors were studied and the results are presented. Although the power delivery network modeling at Intel was very detailed, it is targeted for estimating the IR drop and the worst case switching noise. Therefore the Intel PDN models did not capture the high frequency effects beyond few hundred MHz. Later in this chapter, a comparison of the modeling strategy at Intel and at Dr. Ha's research group is presented. After initial model studies it was decided that the feasibility study with direct high frequency measurements was the best way to show the feasibility of the proposed method.

High frequency measurements were taken on the PDN of Intel's 65 nm Pentium 4 processor and 45 nm Core 2 Duo processor and the results are presented in chapter 4. Measurements were taken on cold as well as active microprocessors. A novel measurement setup was assembled to directly measure the high frequency transfer characteristics of the PDN of a microprocessor in a flip-chip Land Grid Array (LGA) package. This measurement setup is described in detail in this chapter. Attempts were made to answer several supplementary questions as well, i.e. the die-to-die variation, variations based on the location in the die as well as temperature variation of the PDN transfer characteristics.

For further system level study, a channel model was developed based on the measured high frequency transfer characteristics. The details of the channel model are presented in chapter 5. The channel path loss, phase response as well as the impulse response of the PDN channel was extracted from the measurements. To complete the channel model, switching noise in the PDN had to be included. Noise measurements were taken to estimate the typical noise levels in the current generation of Intel microprocessors and the results are presented. The communication link budget was calculated based on the measurements (i.e. channel path loss and noise floor) and appropriate modulation techniques are identified. Other system level issues like the impact of I-UWB pulse shapes on interference to normal operation and mitigation of narrow band interferences resulting from microprocessor operation are discussed as well.

Chapter 6 discusses the circuit design techniques for sending and receiving pulses over the microprocessor PDN. Challenges in transmission and reception of I-UWB pulses in noisy PDN environment are discussed. Simple yet robust digital-process friendly transmitter and receiver designs are proposed. The proposed transmitter and receiver circuits are evaluated through simulations in TSMC 0.18  $\mu\text{m}$  CMOS process and their performance parameters are summarized.

Chapter 7 concludes and summarizes the work presented in this dissertation. The research presented here is a first-of-its-kind proposal and consequently work can be continued in several different areas of concentration. New and exciting applications can be imagined once the communication method is established with a demonstration in an operating microprocessor. Some of these avenues and possible applications are presented towards the end of final chapter.

## **Chapter 2: Preliminaries**

In this chapter, a broad overview of the three major topics which are brought together by the proposal is provided, viz. ultra wideband communication, power line communication, and the power distribution network in microprocessors. First, ultra wideband signaling, advantages of Impulse-UWB signaling, receiver architectures, multiple access techniques and other relevant topics are reviewed. Second, history and communication aspects of power line communications, like the channel modeling, noise issues, transceiver architectures, and applications is reviewed. Last, the overall structure and complexity of the power delivery system of a microprocessor is reviewed. Some relevant noise issues are discussed. The design of decoupling solutions for impedance control of the power distribution network and for reducing the variation in the supply voltage level of the microprocessor is also discussed.

### **2.1 UWB**

#### **2.1.1 Definition**

FCC allowed communication in the UWB spectrum 3.1 – 10.6 GHz. In general, an ultra wideband signal is defined as any modulation scheme where the information bandwidth is 20% of carrier frequency or the absolute bandwidth is at least 500 MHz [5][6]. Figure 2.1 compares the power spectral density of a UWB signal with that of a narrowband and wideband signals. UWB signaling efficiently uses spectrum because the signals may occupy the same bandwidth and coexist with existing narrowband systems.

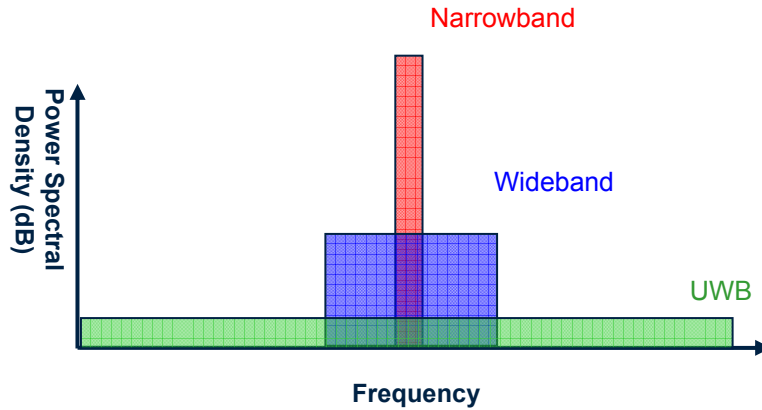


Figure 2.1: Power Spectral Density of UWB, Narrowband, and Wideband

The FCC limits the operating bands for a UWB device according to its application. The rules allow for both unlicensed communications applications and licensed applications such as health monitoring, ground penetrating radar (GPR), and through-walls sensing. Communications systems received license-free spectrum allocation, so anyone anywhere in the United States may use a certified device for communications purposes. These systems operate in the band from 3100 MHz to 10600 MHz. In addition to the average power limits in Figure 2.2; a communications system must also limit its average Equivalent Isotropically Radiated Power (EIRP) to -85.3 dBm/kHz in the frequency bands 1164-1240 MHz and 1559-1610 MHz [5].

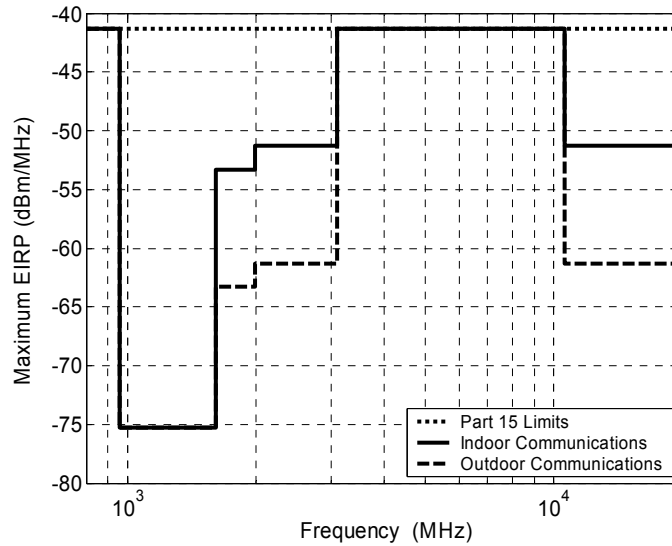


Figure 2.2: Average EIRP Limits for Communications and Measurement Systems

Conveniently, these restrictions do not apply for communication over the power distribution network of a microprocessor. However, the effective radiated power from the power lines must be low enough so as not affect the sensitive analog circuitry in the microprocessor.

### 2.1.2 Signaling for UWB Communications

Two forms of UWB signaling have been pursued recently. They vary mostly in the method used to fill the ultra wideband spectrum because the FCC does not mandate any particular method. At one extreme, a sharp impulse fills the band as in Impulse-Ultra Wideband (I-UWB); and at the other extreme, many simultaneous narrowband tones fill the band as in Multi Carrier - Ultra Wideband (MC-UWB). Many solutions exist in between these extremes - a single band may be divided or notched into a few narrower bands; or, alternatively, several narrow bands may combine to fill large bands in the spectrum. The solutions may or may not utilize a carrier frequency. The two

leading proposals for UWB standardization, direct sequence UWB (DS-UWB) and Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) [7]-[9].

Traditional narrowband radio systems modulate data onto a carrier signal to occupy a narrow frequency band of a few KHz to a few MHz, but the signal is continuous in time. The unique signaling of I-UWB represents the dual of narrowband signaling. A narrow pulse may occupy several GHz of spectrum, but it may last only a few hundred picoseconds. The Pulse Repetition Interval (PRI) is generally much larger than the pulse width, i.e. an I-UWB pulse train has a small duty cycle ( $\ll 1$ ). The inverse of the PRI is the pulse repetition frequency (PRF).

Common pulse shapes for I-UWB communications are derived from the Gaussian pulse [10][11]. Derivatives have decreasing bandwidth and increasing center frequency. By shaping the pulse, the spectrum of the pulse can be placed in the frequency band for communication over the power distribution network. Figure 2.3 shows the Gaussian pulse, its first derivative (a Gaussian monopulse), and its second derivative (a Gaussian doublet) in both the time and frequency domains.

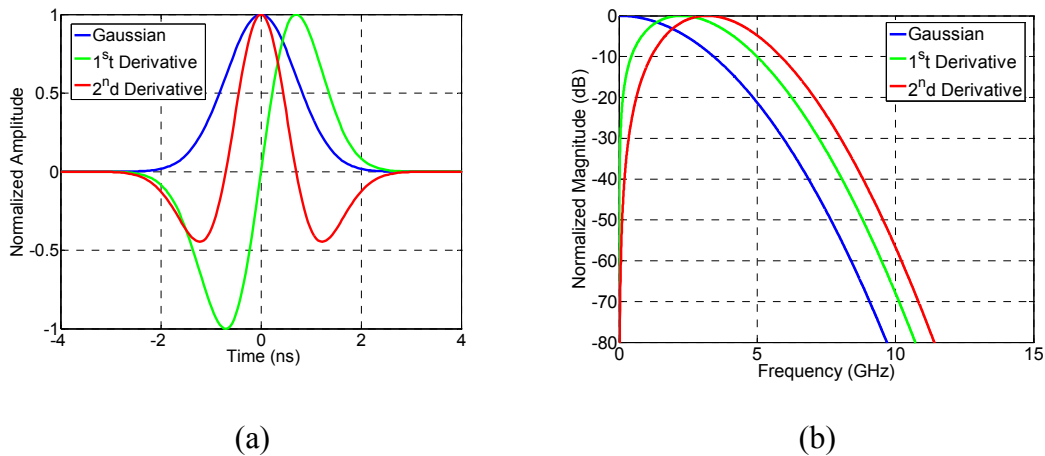
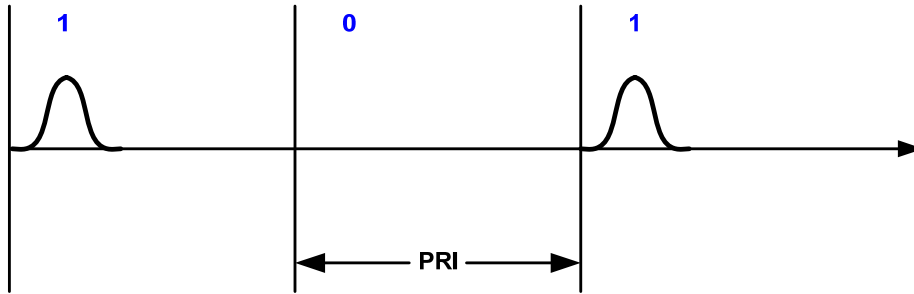


Figure 2.3: Gaussian pulses and their spectrum

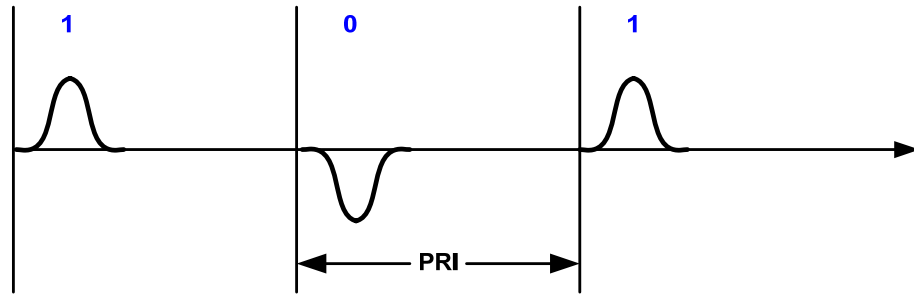
### 2.1.3 Modulation Techniques

In the world of wireless communication, UWB is considered an attractive technology for its high capacity, high data rates, robustness against fading, low power consumption, low cost and low-complexity devices [12]. In spite of all the benefits of UWB, the extremely wide frequency bands (at least greater than 500 MHz) and exceptionally narrow pulses (in the range of few hundred picoseconds) make it difficult to apply conventional narrowband modulation techniques into UWB systems.

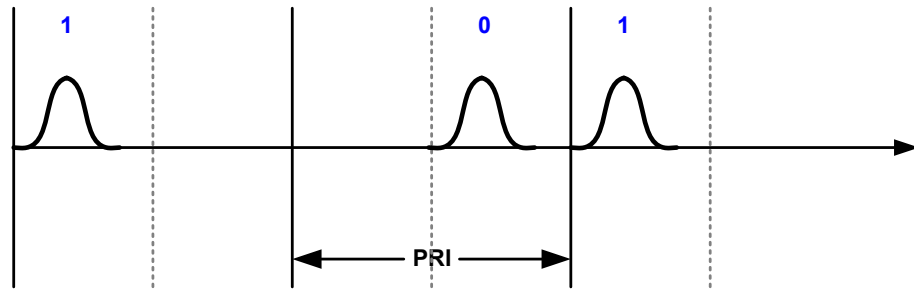
There are various possible modulation options that depend on the application, design specifications and constraints, range, transmission and reception power, quality of service requirements, regulatory requirements, hardware complexity, data rate and reliability of channel, and capacity [13]. Therefore it is crucial to choose the right modulation for the right purpose. Some of the well-studied modulation schemes in UWB are BPSK, QPSK, PAM, OOK, PIM, and PSM [14]. The OOK, BPSK, PPM and PSM modulation techniques are illustrated in Figure 2.4. Of these options, BPSK is one of the most popular modulation schemes in UWB applications due to its smooth power spectrum and low BER. Compared with BPSK, OOK and PPM only require the knowledge of the presence or absence of signal and therefore channel estimation is not necessary. In PSM, a different pulse shape is transmitted depending on the digital information and has been shown to be robust in the presence of clock jitter [15][16]. The noise level in wireless channels also influences the choice of modulation. Higher-order modulation schemes ensures high data rate at the cost of poor BER in a noisy channel. Therefore, lower order modulation for low-data-rate applications is desired in poor channel conditions. One can also consider transmission over multiple frequency bands or over multiple carriers, and various multiple accessing options such as Time-Hopping and Direct-Sequence under the umbrella of UWB modulations [17][18].



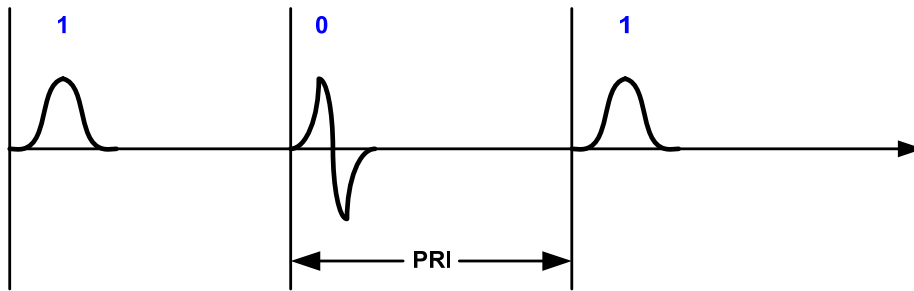
(a) OOK



(b) BPSK



(c) PPM



(d) PSM

Figure 2.4: Modulation Techniques for I-UWB

## 2.1.4 Advantages of UWB Signaling

Compared to narrowband systems, UWB has several advantages. Because of the combination of wide bandwidth and low power, UWB signals have a low probability of detection and intercept [14][19]. Additionally, the wide bandwidth gives UWB excellent immunity to interference from narrowband systems and from multipath effects. Another significant advantage of UWB is its high data rate. Figure 2.5 shows that a high data rate is more easily achieved by increasing bandwidth than by increasing SNR. This is a consequence of Shannon's channel capacity theorem, which states that channel capacity increases linearly with bandwidth, but increases only with the  $\log_2$  of the SNR [20]. In Figure 2.5, theoretical data rates of over 500 Mbps are achieved easily by a UWB system in a low-SNR environment, but such data rates are nearly impossible for the narrowband systems in the figure. This makes it highly suitable for high data rate applications and for our proposed method based applications because the additional noise added by UWB signaling is very low by design.

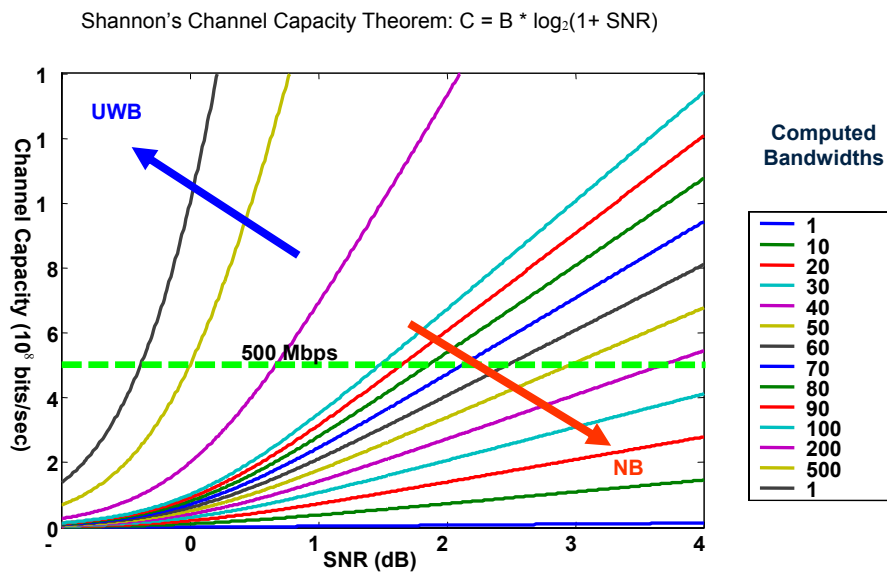


Figure 2.5: Channel Capacity of UWB versus Narrowband

Furthermore, UWB is essentially an overlay technology that is inherently designed to have low radiated power and to coexist with both narrowband

systems and other UWB systems. This property helps to reduce the interference caused by the proposed communication method to the normal operation of the microprocessor. In addition, I-UWB is relatively immune to multipath induced fading effects in both indoor and outdoor environments. The multipath fading effects help in the transmission of UWB pulses through the branched grid structure of the power distribution network. The wide instantaneous bandwidth increases the number of resolvable multipaths and results in robustness to harmful multipath effects [11]. The wide instantaneous bandwidth also enables fine time resolution for use in more conventional applications like radar, imaging, and ranging.

Finally, the carrier less nature of I-UWB gives it potential for simple circuit implementations without intermediate oscillators and mixers [21]. UWB transceivers could have a nearly all-digital implementation in CMOS with minimal analog RF electronics [22][23]. This simple architecture can translate to low power dissipation low cost, and wide deployment of I-UWB receivers at different internal nodes in a microprocessor.

## **2.1.5 I-UWB Receiver Architectures**

### **2.1.5.1 Optimal Matched Filter**

In matched filtering, the basic principle is to estimate the noiseless replica of the received waveform and to use this estimate as a filter to maximize the SNR at the output of the matched filter [20]. The structure of an optimal matched filter based receiver is shown in Figure 2.6. In AWGN channels (assuming no other user's interference and self interference), the matched filtering provides an optimal receiver in the sense that it minimizes the probability of error. The matched filter can be implemented in a rake receiver (multiple parallel correlators and optimal combining) structure [14][24].

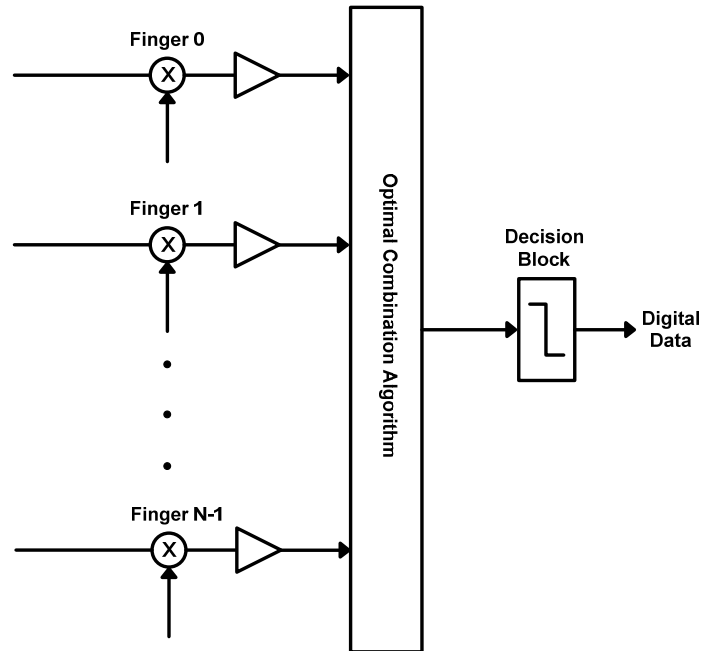


Figure 2.6: Optimal matched filter based receiver

### 2.1.5.2 Transmitted Reference (TR) Based Scheme

The basic principle in TR-based schemes is to transmit a reference (unmodulated) pulse along with the data (modulated) pulses. The reference pulses and the data pulses are transmitted with a delay and data pulses can be assumed to be affected similarly due to the channel. The structure of a TR-based I-UWB receiver is shown in Figure 2.7. Therefore, unlike the matched filtering case, instead of using a local template, the TR scheme uses the reference pulses as the template for correlating the data pulses, and for the demodulation of the transmitted information. In this way, explicit channel parameters estimation is not needed at the receiver. As a result, TR communication possesses some advantages when transmitting through an unknown channel, which severely distorts the transmitted waveforms. The TR-based scheme has the ability to capture the energy from all multipath components of the received signal with a simple receiver structure. However, the gain comes at the expense of a higher noise power,

due to the structure of the TR receiver, but the trade-off is advantageous in an environment with sufficiently high and dense multipaths.

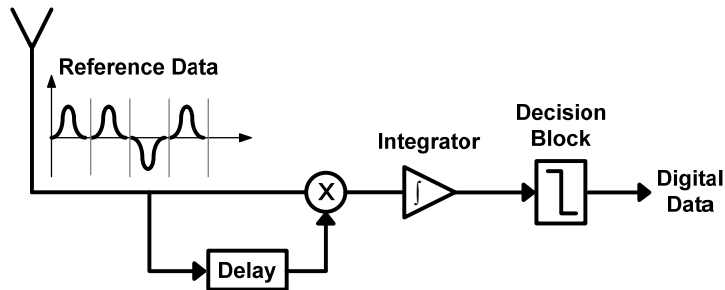


Figure 2.7: Transmitted reference based receiver

### 2.1.5.3 Differential Detector

The differential detector is similar to the TR scheme. Instead of sending reference pulses for correlating the received signal, the data pulses corresponding to the previous symbol are used as the template. This requires differentially encoding the transmitted bits before modulation, so that the information is in the difference of the two consecutive symbols. Avoiding the use of reference pulses in differential detectors increases spectral efficiency and hence doubles the data rates compared with the TR scheme. One major disadvantage of a differential detector is that it is very sensitive to timing and delay errors. Even a slight difference in delays will degrade the performance of the receiver significantly. Also the channel is assumed to be time invariant over the duration of two consecutive symbols. For high mobility and large symbol duration, differential detectors may not be an appropriate choice.

### 2.1.5.4 Energy Detector

An energy detector is a simple suboptimal non-coherent receiver scheme. An energy detector receiver is shown in Figure 2.8 [14]. A threshold must be set and used, where the bit decision is ‘0’ if the received energy is less than the threshold and ‘1’ if it is larger than the threshold. The optimum threshold is the intersection of the probability density functions corresponding to energies for ‘0’ and ‘1’. Similar to the TR scheme, the UWB energy detector receiver approach requires only coarse synchronization, which makes the system robust against clock jitter. It is also not sensitive to distortion and phase nonlinearity of devices like antennas, amplifiers or filters. The integration interval in an energy detector receiver can be adapted depending on the maximum excess delay of the communication channel. Choosing an integration interval that sacrifices the insignificant multipath components in order to decrease the collected noise energy will improve the performance. Depending on the SNR and multipath delay profile, the optimal integration interval changes. The output of the integrate and dump circuitry for each symbol in the energy detector can be written as

$$y_j = \int_{\tau}^{\tau+T_0} [\beta_j s(t) + n(t)]^2 dt$$

$$y_j = \beta_j^2 \int_{\tau}^{\tau+T_0} s^2(t) dt + 2\beta_j \int_{\tau}^{\tau+T_0} s(t)n(t) dt + \int_{\tau}^{\tau+T_0} n^2(t) dt \quad (2.1)$$

where  $s(t)$  is the noiseless received signal,  $\beta_j$  is the modulated symbol,  $T_0$  is the integration interval, and  $\tau$  is the starting point of the integration.

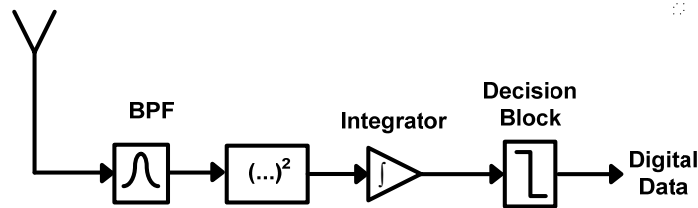


Figure 2.8: Energy detector receiver

## **2.1.6 Effect of Narrowband Interference on UWB**

### **2.1.6.1 Sources of Interference**

The very low transmission power and large bandwidth enable UWB systems to co-exist with other narrowband systems without interfering with them. However, the effect of the narrowband signals on the UWB signal can be significant and may jam the UWB receiver completely. There are three major sources of interference in UWB viz. the Intersymbol Interference (ISI), Narrowband Interference (NBI) and Multiple Access Interference (MAI) [26]. ISI is mainly a problem in high data rate systems, where the multipaths interfere with consecutive symbols. NBI is caused by the existing narrow band systems in their previously allocated bands. MAI is caused by several users operating over the same band as in Code Division Multiple Access (CDMA) detailed later in section 2.1.7. The coexistence of a large number of UWB transmitters in a dense environment is very important. The transmitted signals of each user share the same spectrum, and simultaneous transmissions by multiple users are popularly achieved by TH and DS spreading codes. Ideally, it is desired to have orthogonal codes for each user. However, in practice, the received signal from different users is not orthogonal because of multipath, asynchronous transmission. Also, designing perfect codes with zero auto and cross correlation properties for all shifts is not possible. As a result, MAI in UWB communication systems is a major problem.

### **2.1.6.2 Interference Avoidance**

Equalizers can be mainly used to handle ISI and by simply allowing sufficient guard interval which leads to reduced data rates. Simple and efficient equalization techniques borrowed from narrowband systems can be employed for UWB as well. The current trend in NBI is to avoid transmission of the UWB signal over the part of frequency where NBI is strong. Analog bandpass filtering before the reception of the signal, notch filtering and peak clipping, and Minimum Mean Square Error (MMSE)

combining are some of the approaches that are considered for cancelling NBI [108]. The effectiveness of interference cancellation depends on the ability to separate the desired signal from the interferer(s). Approaches that use Minimum Mean Square Error (MMSE) combining of rake fingers and techniques that are used for conventional CDMA can also be used for UWB [14].

## **2.1.7 Multiple Access Schemes**

### **2.1.7.1 Time Division Multiple Access (TDMA)**

The time division multiple access (TDMA) scheme is a transmission technology that allows a number of users to access a single channel (originally radio frequency channel) without interference by allocating unique time slots to each user within a channel. TDMA can fail to transmit or receive due to occupancy problem, sensitivity to multipath interference, and high cost compared with that of CDMA (Code Division Multiple Access)

### **2.1.7.2 Code Division Multiple Access (CDMA)**

CDMA is a digital cellular technology that uses spread spectrum techniques. Unlike competing systems, such as GSM (Global Systems for Mobile Communications) that use TDMA, CDMA does not assign a specific time or frequency channel to each user. Instead, every channel uses the full available spectrum. Individual communications are encoded with a pseudo-random digital sequence. Different code channels, ideally orthogonal to each other, allow simultaneous transmission for multiple users. With this structural support for no collisions, users avoid the overhead of handshaking and detecting medium activity. In I-UWB, the channel may be divided into code spaces by employing time hopping codes or direct sequence codes [25].

Time-hopping is the most well-known form of code division for I-UWB signals. The  $k^{th}$  user transmits the signal

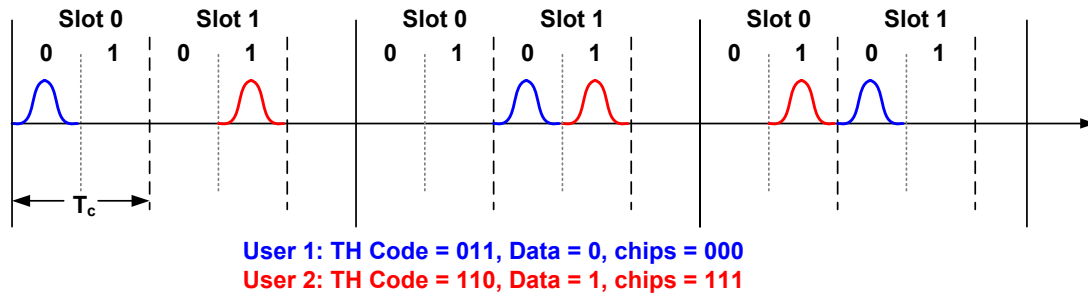
$$s^{(k)}(t) = \sum_{i=-\infty}^{\infty} A_p \left( t - iT_f - c_i^{(k)}T_c - \delta d_{\lfloor \frac{i}{N_c} \rfloor}(t) \right) \quad (2.2)$$

with time-hopping code  $c_i^{(k)}$  and chip duration  $T_c$ . Figure 2.9 shows time hopping for a length  $N_c = 3$  code. Figure (a) shows the spreading over the hopping codes for both users; User 1 transmits a data '0' and user 2 transmits a data '1'. The time hopping code determines the slot number and the data determines the pulse position within that slot. Note that pulses from two different users may interfere with each other in the same slot (as in the second chip), but spreading multiple data chips over a code mitigates such multiple access interference.

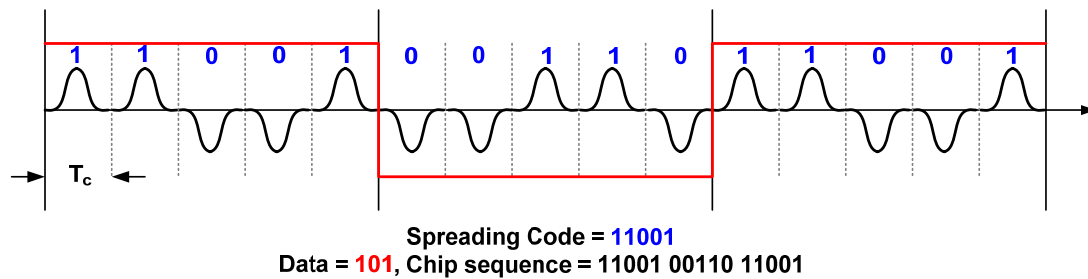
Direct sequence UWB (DS-UWB) is similar to well-know narrowband direct sequence spread spectrum techniques, but I-UWB communication systems spread the signal in time as opposed to frequency. A user transmits a train of data with the amplitudes of the chips modulated by the spreading code. The DS-UWB waveform for the  $k^{th}$  user in Figure 2.9 can be represented as

$$s^{(k)}(t) = \sum_{i=-\infty}^{\infty} \sum_{j=1}^{N_c} A_p (t - iT_f - jT_p) (C_j^{(k)}) d_i(t) \quad (2.3)$$

with spreading code  $c_j^{(k)}$  for the  $j^{th}$  pulse in a length  $N_c$  code.



(a)



(b)

Figure 2.9: Time hopping vs. direct sequence multiple access

## 2.1.8 Applications

Since 2002, UWB has generated tremendous interest, and many new ideas for applications have come from both industry and academia. The radar capability and flexibility in data rate and link distance open the possibility of many new applications not suitable for narrowband systems.

### 2.1.8.1 Radar

I-UWB has been naturally suitable to radar applications with wide bandwidth and low duty cycle. The wide bandwidth identifies more target information, improves range accuracy, improves resilience to passive scatterers, mitigates destructive multipath effects from ground reflection, and enables a narrow antenna beam pattern. The low

radiation power under the spectral mask provides a low probability of intercept and detection. Pulses with low center frequency (and thus a significant portion of power in the large wavelength) can be used to penetrate solid structures such as concrete walls. I-UWB can provide one low-cost interface for both a sensor and a communication system. With these advantages, I-UWB can be applied to vehicular radar, ground penetrating radar, through-walls imaging, and medical imaging [27][28].

### **2.1.8.2 Communications**

Recent applications of communication using UWB signaling focus on short-range, high-rate wireless communications such as Wireless Personal Area Networks (WPANs), which construct a network with a limited number of devices in a small coverage area (within 10m) [29]. The proposals for the IEEE 802.15.3a standard defined medium access and physical layers with extremely high data rates (up to Gbps) for multimedia applications. The most common application for WPAN is cable replacement for high data-rate devices such as video players and PC wireless USB devices. Another cable replacement application is wearable peripherals for health, entertainment, or military purposes with support of Body Area Networks (BANs) [30].

### **2.1.8.3 Location Aware Communications**

With the dual use of the above two conventional applications of radar and communications, I-UWB offers communications with location awareness [31][32]. I-UWB can have ranging capability with sub-centimeter accuracy even at low SNR with possibly one transceiver. Nodes can also share distance estimates to cooperatively compute location information, which is an important feature for many sensor network applications and network protocols [33].

#### **2.1.8.4 Sensor and Ad Hoc Networks**

Many recent applications of UWB are in the area of ad hoc and sensor networks. While ad hoc and sensor networks have been steadily investigated in the literature of several years with a narrowband perspective. Ad hoc and sensor networks can utilize the location awareness of UWB for networking in a sensor field without existing infrastructure, i.e., the network is responsible for self-configuration [33]. For sensor networks, power consumption, cost, and Quality of Service (QoS) are crucial design factors for the Physical layer (PHY) and Medium Access Control (MAC) protocol [34][35].

## **2.2 Power Line Communications**

In this section, we review the history of power line communications, noise issues as well as signaling and the channel modeling of the power lines for data communications.

### **2.2.1 Power distribution and the History of PLC**

Figure 2.10 shows the different layers in the power distribution. The VL model has four voltage layers, EHV, HV, MV, and LV (Extremely High Voltage, High Voltage, Medium Voltage and Low Voltage) with intermediate transformers. The high voltage power lines or even extremely high voltage power lines emanate from power plants and represent a wide-meshed long-distance nationwide network. The term HV applies to voltage over 36 kV, EHV to voltage over 300 kV. The next lower level is constructed for delivering power into cities, towns, and villages. The term ‘medium voltage’ covers the range from 1 kV to 36 kV. Eventually, MV is transformed down to low voltage with levels below 1 kV for distribution to customer premises as shown in Figure 2.10 [36]. The LV varies depending upon the consumer load. The power line communications is usually conducted over the medium and low voltage power lines are the ‘last mile’ communications.

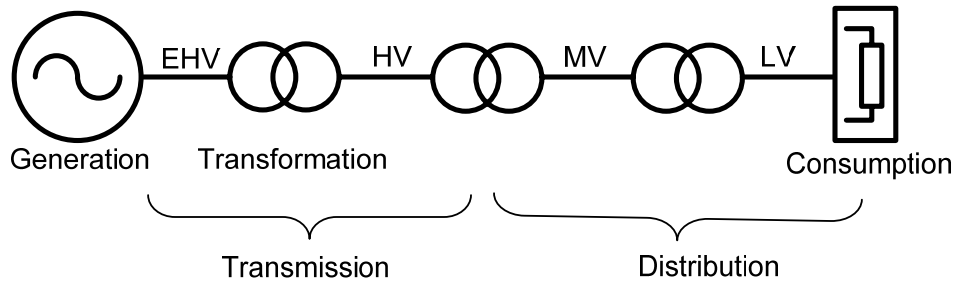


Figure 2.10: Voltage layers in Power line Communications

Power line communications, using power lines for dual purposes of data communications, was patented in the early 1920's [36][37]. The utility companies planned from the very beginning to build their own data networks for information transmission. The general telephone network was found to be unsuitable, particularly for telemetering and remote monitoring, because it is not available anywhere, and even very short interruptions can have dangerous consequences. In addition, the use of leased lines would not be economical for large distances. Electric supply companies used data networks over power lines for operations management, monitoring and limitation and removal of failures [38]. Recently, it has been revived for broadband internet access over existing power lines under the name Broadband over Power Lines (BPL) [38]-[41]. PLC also applies to narrowband applications within the frequency range of few kilohertz.

The main advantage of PLC is to utilize the existing resources for communication purposes, i.e. 'no new wires' for data transmission. The other advantage is the extension to wide area networks, since power lines offer a convenient and inexpensive shared medium for data transmission. Although, there are apparent advantages in the nation-wide power supply networks, there are several challenges for the large scale deployment of PLC. They mainly result from the fact that data transmission should not disturb the main function of power delivery as well as not violate regulatory concerns [42].

Recently, there have been major developments in the standardization of power line communications and products have been introduced in the market by major players

like Siemens, Texas Instruments, Sony, Mitsubishi and Panasonic. HomePlug Power Alliance Inc., was formed in March 2000 by 13 founding members [36]. HomePlug is a non-profit corporation formed to provide a forum for the creation of an open standard and specification for home powerline networking products and services and to accelerate the demand for products based on these standards worldwide through the sponsorship of market and user education programs. In addition, European Telecommunications Standards Institute (ETSI) has initiated a PLC project to develop standards and specifications and provision of voice and data services over the mains power transmission and distribution network and in-building electrical wiring.

### **2.2.2 Channel modeling for power line communications**

For any communication system evaluation, an appropriate channel model is crucial for the evaluation of its performance. However, there has been no standardized channel model for PLC channels due to the difficulties of characterizing the power supply network. Channel modeling for PLC suffers from a number of technical challenges [36];

- Frequency varying and time-varying attenuation
- Dependence on location, network, topology, and connected loads
- High interference due to noisy loads
- Highly colored background noise
- Various forms of impulse noise
- Electromagnetic Compatibility (EMC) issues that limit available transmitted power

The most popular channel model for the power line is the echo-based transfer function model approach proposed by Dostert et. al. [43][44]. Attenuation increases with frequency in most long-distance powerline links. A low pass characteristic can also be observed in a less significant form on indoor links. In addition, periodic

fluctuations can be ubiquitously discerned, suggesting the following echo based transfer-function model approach as shown in Figure 2.11.

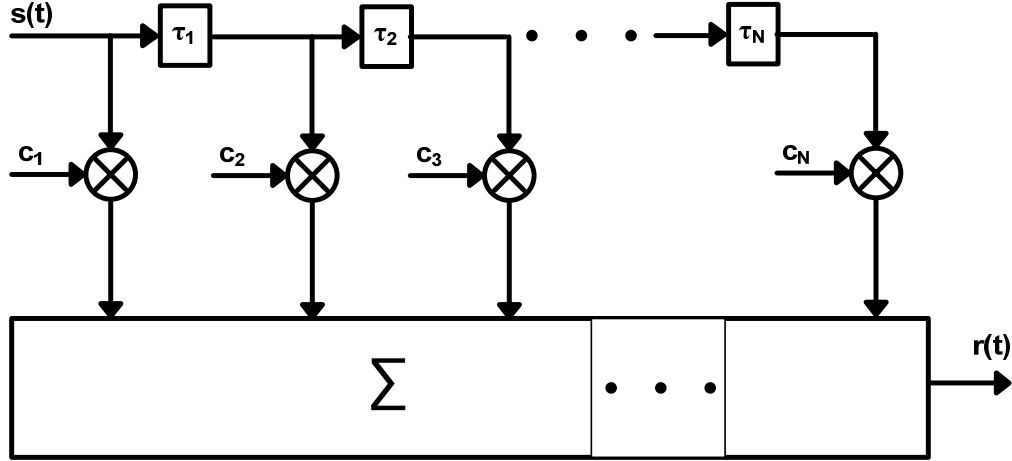


Figure 2.11: Echo channel model for the power line

The basic behavior a transmission channel incorporating  $N$  echoes can be described by an impulse response

$$h(t) = \sum_{i=1}^N c_i \delta(t - \tau_i) \quad (2.4) \quad ,$$

where the coefficients  $\tau_i$  denote the echo delays and the factors  $c_i$  stand for the echo attenuation. From (2.4), the transfer function

$$H(f) = \sum_{i=1}^N c_i e^{-j2\pi f \tau_i} \quad (2.5)$$

be calculated. Under the real-world conditions, however the coefficients  $c_i$  depend not only on the cable length, but also on frequency. Based on numerous channel investigations, the following expression is finally found:

$$c(f, l_i) = a_i \cdot e^{-\alpha(f) l_i} \quad (2.6)$$

In (2.6)  $l_i$  for the cable length and  $a_i$  is a specific weighting factor regarding network topology details;  $a_i$  represents the product of reflection and transmission factors along the  $i^{th}$  echo path. Combining multipath propagation and frequency-and-length-dependent attenuation, and introduce phase velocity  $v_p$ , finally leads to the complete transfer function.

$$H_E(f) = \sum_{i=1}^N a_i e^{-\alpha(f)l_i} e^{-j2\pi f \frac{l_i}{v_p}} \quad (2.7)$$

The coefficient  $\alpha(f)$  needs further explanation; Based on an analysis using the physical cable parameters resistance per meter ( $R'$ ), lateral conductivity per meter ( $G'$ ), inductance per meter ( $L'$ ), and capacitance per meter ( $C'$ ), we can derive the following result for the complex propagation factor:

$$\gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')} = \alpha + j\beta \quad (2.8)$$

Under the assumption that  $R' \ll \omega L'$  and  $G' \ll \omega C'$  in the frequency range of interest, a cable can be considered as weakly lossy and hence the following approximation is valid:

$$\gamma = \underbrace{\frac{1}{2} \frac{R'}{Z_L} + \frac{1}{2} G' Z_L}_{\text{Re}(\gamma) = \alpha} + \underbrace{j\omega \sqrt{L' C'}}_{\text{Im}(\gamma) = \beta} \quad (2.9)$$

with

$$\alpha(f) = \frac{1}{2} \frac{R'}{Z_L} + \frac{1}{2} G' Z_L \approx \vartheta_1 \cdot \sqrt{f} + \vartheta_2 \cdot f \quad \text{and} \quad \beta = \omega \sqrt{L' C'} = \frac{\omega}{v_p} \quad (2.10)$$

Here  $R'/2Z_L$  describes the impact of the skin effect, and  $G'Z_L/2$  denote the dielectric losses within the insulation material. A further approximation step leads to the expression (2.11)

$$\alpha(f) = (\eta_0 + \eta_1 \cdot f^\varepsilon) \quad (2.11)$$

which turns out to be advantageous for setup and handling of the echo model in practice, because the coefficients  $\eta_0$ ,  $\eta_1$ , and  $\varepsilon$  are generally constant for a cable type, and  $\varepsilon$  stays in a quite narrow range between 0.5 and 0.7.

### 2.2.3 Interference and noise issues in PLC

An overview of the interference and noise issues in PLC is shown in Figure 2.12. Interference and noise in PLC can in general be classified into three general cases: colored background noise, narrowband interference, and impulsive noise.

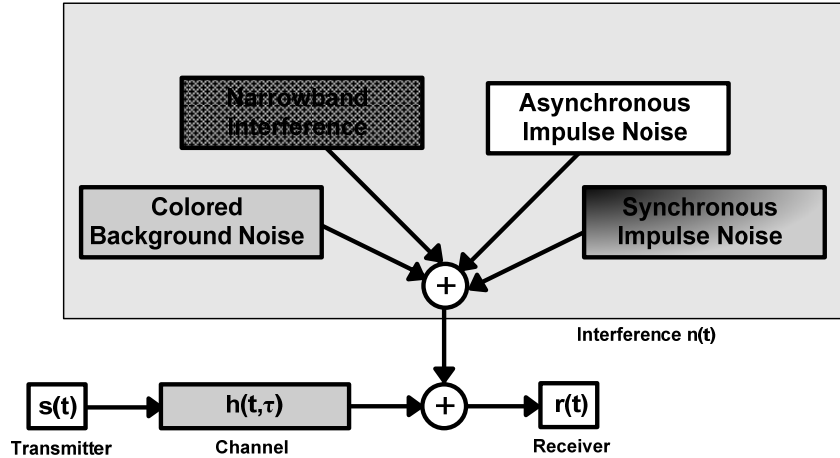


Figure 2.12: General interference and noise in PLC

Normally, the root mean square (rms) amplitude of the first two types varies slowly over time. So they can be summarized as background noise. On the other hand, the last three types can be regarded as impulsive noise since their amplitudes change rapidly. Since the impulsive noise is actually produced by appliances in the power network, the power-line noise can also be regarded as a combined sum of the background noise and the impulsive noise from all nearby appliances. During the occurrence of impulses, the noise PSD rises perceptibly and may cause bit or burst errors. The three different classes of interference are explained in more detail below,

### 2.2.3.1 Colored Background Noise

This kind of interference is of stochastic nature and can be described by a Power Spectral Density (PSD). High PSD values are characteristic for networks, starting from the power frequency (50 to 60 Hz) to frequencies of about 20 kHz. A continuous decrease of the power spectral density is observed above those values as the frequency rises. At 150 kHz, there is often only 1/1000 of the value found at 20 kHz. Towards even higher frequencies there is only background noise with very low power spectral density, which is normally called white noise.

### 2.2.3.2 Narrowband Noise

Narrowband noise, mostly amplitude modulated sinusoidal signals caused by ingress of radio broadcasting stations. Narrowband interference at frequencies below 150 kHz i.e., below the radio frequency bands can originate from switching power supplies, frequency converters, fluorescent lamps, or television sets and computer screens. At the higher frequencies, most narrowband interference comes from radio stations.

### 2.2.3.3 Impulsive Noise

Impulsive noise is characterized by short voltage peaks that last about 10 - 100  $\mu$ s and can reach beyond 2 kV. Basically these are rare single events, which are caused by on and off switching events, and they are different from frequently occurring periodic events. Periodic impulses are mostly caused by phase controls, (e.g. light dimmers) and occur during each zero-crossings of the network voltage i.e., with a frequency of 100 Hz. Impulsive noise can further be classified into the following three different types;

- Periodic impulsive noise *asynchronous* to the mains frequency, which is mostly caused by switched-mode power supplies.
- Periodic impulsive noise *synchronous* to the mains frequency, which is mainly caused by switching actions of rectifier diodes found in many electrical applications
- Asynchronous impulsive noise, which is caused by switching transients in the power network

Depending on the duration of this interference, one or several bits in a data transmission can be corrupted. Such errors have to be prevented by suitable channel coding measures.

## **2.2.4 Powerline Modems**

A complete node for power line communications is presented in [45]. An inductive interface is used to extract the signal from the power lines. The SOC also includes an 8051 microcontroller, a medium access controller UART (MAC) and a modem circuit to comply with the European Home Systems specifications (EHS) for the power line medium. Two data rates 2.4 Kbps and 1.2 Kbps are supported according to the EHS specifications. A spread spectrum based baseband transceiver for a powerline modem is described in [46]. The modem uses M-ary Bi-Orthogonal Keying (MBOK) and provides 128-Kbps data rate. Texas Instruments (TI) promotes the TMS320C2000 series of digital signal controllers as an ideal platform for power line networked applications. TI also provides a free PLC software library and a hardware reference design for data throughput of up to 5 Kbps. TI's partner's Adaptive Networks, Inc., deploys commercial systems that provide up to 100 Kbps throughput and a range of several kilometers [47].

## **2.2.5 Applications for PLC**

Worldwide, there is an ever-growing interest to squeeze more and more data capacity out of indoor installations. Other than wireless approaches such as DECT (Digital Enhanced Cordless Telecommunications) or Bluetooth, there are very few alternatives except additional wiring. Power line is not challenged by walls and other obstacles because the signals mainly run along the wires and the coverage is perfect even for large buildings. Power line communications has possibilities for automation and entertainment, not only in industrial or commercial environments but also for the individual customer. Power line communications can also be used in in-house communication between different rooms in the house. The existing powerline in a house can also be used as a Local Area Network (LAN) backbone. Computers, modems and telephones can thus communicate with one another through this network. These data transmission applications and network operations essentially require reliable

and high-speed communication capability. Though powerline channel does not offer perfect communication quality for large and sophisticated network operations, it provides a sufficient and low-cost solution to in-house data communication applications.

Besides power line communications and ADSL (Asymmetric Digital Subscriber Line), other last-mile solutions have been proposed by the industry and different service providers. For example, cable television channels could be shared to a certain extent. Appropriate systems and devices have already been developed. However, such a solution has serious disadvantages in comparison with PLC. On the one hand, substantial portions of cable TV networks still are owned by the former monopolists, and on the other hand, expensive changes will be necessary. In contrast, power supply networks need only slight modifications, and these networks are ubiquitous all over the world.

### ***2.3 Power Distribution Network (PDN) in Microprocessors***

In this section, the structure and design of power distribution network in microprocessors is reviewed.

#### **2.3.1 Architecture of the Microprocessor PDN**

The microprocessor PDN consists of interconnect networks with decoupling capacitors on a printed circuit board, an integrated circuit package, and the die. It supplies power depending on the performance, size and cost characteristics of the overall electronic system. The power delivery system of a microprocessor is shown in Figure 2.13. The components in the power supply system are connected through several layers of packaging hierarchy with multiple power and ground planes. First, we consider the voltage switching regulator module converts one DC voltage to another, for example 5-1.2 V, which is usually in an off-chip environment. The regulator functions as the powers source and the integrated circuit will be the power load (or

sink). There must be sufficient capacitance in the PDN to supply the current and supply voltage until the VRM can respond. Decoupling capacitors are used to reduce the impedance of the PDN and the switching noise in the PDN. Decoupling of PDN will be discussed later in section 2.3.3.

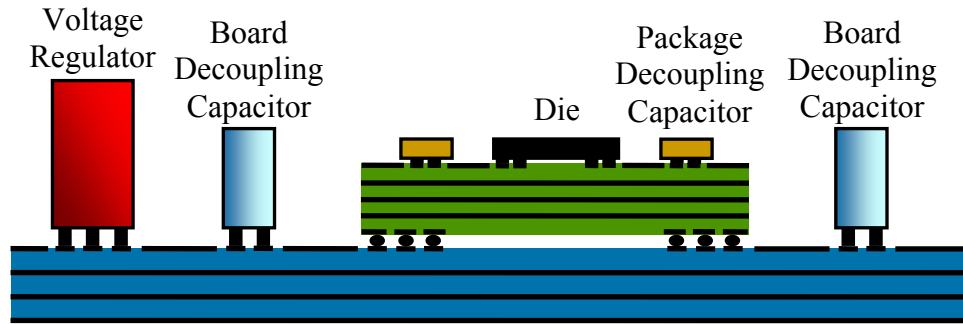


Figure 2.13: Microprocessor power distribution network

The on chip power grid is designed as a branched grid structure to cover the entire microprocessor die. An on-chip power grid is shown in Figure 2.14. When deciding the width of the metal lines in the on-chip power grid particular attention is paid to reliability of the metal lines (i.e. electromigration effects).

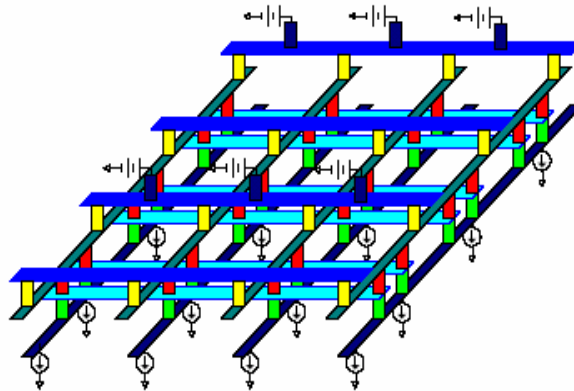


Figure 2.14: On-chip power grid in a microprocessor

Electromigration in an IC is the movement of metal ions as the result of flow of electrical charges through the metal lines in the chip, particularly the metal lines that

distribute power within the chip [48]. This unwanted metal ion movement could open up metal voids in some parts of the wires and build up metals at other sites. At the sites from which metal migrates, voids increase the resistance of the affected wire and, in extreme cases, can cause it to break down completely. At the receiving end of the electron migration, the buildup of metal can form hillocks that, in extreme cases, can span the gap between adjacent wires and cause shorts between them. The increase in resistance caused by electromigration appears only after a period of incubation. During this period, wire resistance remains fairly constant. After that, it increases steadily, eventually causing the IC to fail. The period of incubation depends on metal line size and current density. Current density can be reduced by increasing the size of the metal lines or adding more contacts between metal lines. Adding more power lines on metal layers also reduces the current densities.

In general, with more metal lines and vias used in the power distribution network, the electromigration failures are decreased. As the width is increased, the capacitance loading of the metal line increases but the resistive drop in the metal line also decreases. When choosing the metal spacing, and the metal width, inductance introduced is also considered carefully. The first order estimation of unit-length loop inductance for adjacent power and ground lines is given in (2.12).

$$L = \mu \frac{s}{w} \quad (2.12)$$

### 2.3.2 PDN - Design Philosophy

The design of PDN for microprocessors has become an increasingly difficult challenge in modern CMOS processes [49]. The main intent of the PDN design is to reduce the voltage variations from current transients by keeping the overall impedance of the PDN to a minimum. To this end, the target impedance of a PDN can be expressed as shown in (2.13),

$$Z_{target} = \frac{V_{dd} \times r}{I} \quad (2.13)$$

where  $V_{dd}$  is the power supply voltage,  $r$  is the allowable ripple voltage and  $I$  is the current. With general scaling trends, the current  $I$  is increasing and the power supply voltage  $V_{dd}$  is decreasing. Therefore, the target impedance of the PDN is falling at an alarming rate, a factor of five per computer generation [49][50]. The specific impedance must be satisfied not only at DC, but also at all frequencies where current transients exist [51].

Typically,  $\pm 5\%$  of the nominal supply voltage  $V_{dd}$  is fixed as the upper and lower thresholds for maximum allowed variations on the supply voltage. An illustration of the variations in the  $V_{dd}$  voltage is shown in Figure 2.15.

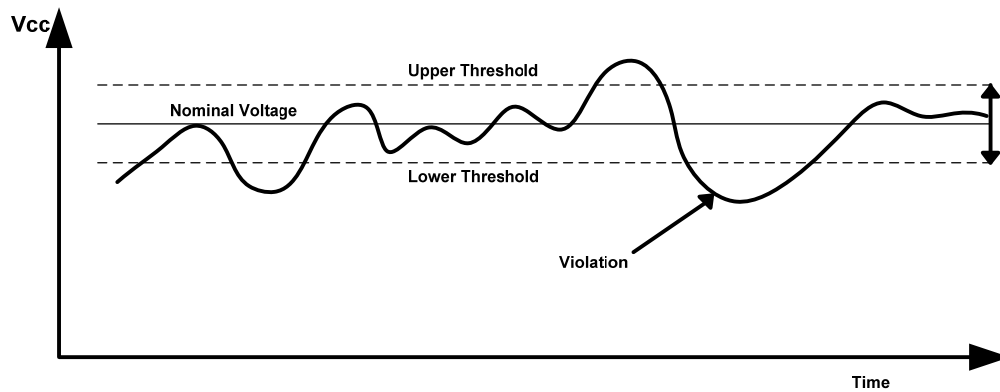


Figure 2.15: Variation of PDN voltage

Switching noise in the PDN is caused by the currents drawn by the switching circuits in a microprocessor die. The current transients lead to voltage drops over the resistance of the interconnection network (IR drop). Additionally, the fast switching currents have a large  $di/dt$  which creates a large voltage drop in the inductive elements of the PDN. Since the switching activity taking place in a die is enormous, switching activity can only be characterized by statistical means and hence the resulting power supply appears as random noise [52]. Characterization, modeling and measurement of on-chip power supply noise will be detailed in chapter 5 of this thesis.

### 2.3.3 PDN Impedance Control and Switching Noise Reduction

Decoupling capacitors serve multiple purpose, they are used for reducing the slew rate of current variations by locally supplying currents to the switching circuits, to dampen resonances in the power supply impedance and to reduce the overall impedance of the power distribution network over the frequencies of interest i.e. from DC to the maximum clock frequency of the microprocessor [49][53][54]. The typical impedance profile of a microprocessor PDN is illustrated in Figure 2.16. Positive and negative peaks occur in the PDN impedance characteristics due to the resonance and antiresonance phenomenon occurring between the different inductance and capacitance elements in the PDN respectively.

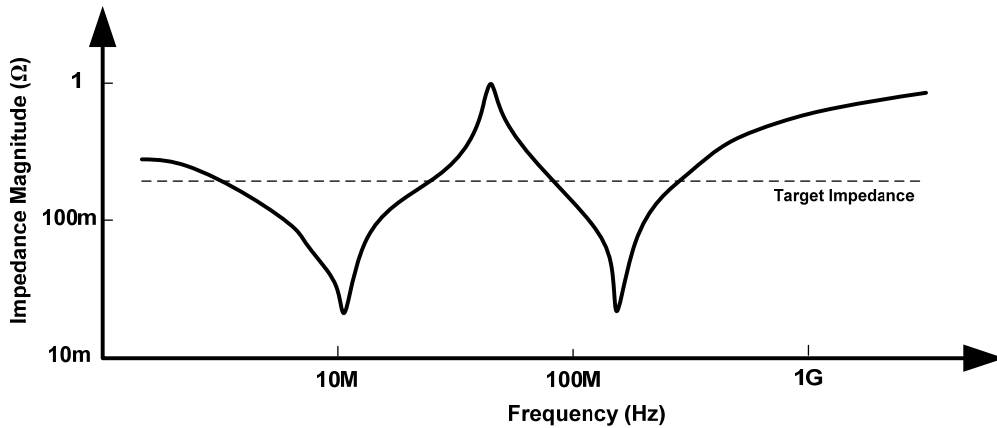


Figure 2.16: Illustration of resonances of the PDN impedance

In Figure 2.16, the two negative peaks correspond to the resonance between the inductance in the power planes and different decoupling capacitors in the PDN. Decoupling capacitors of widely differing values are used in the PDN to reduce the power supply noise in different frequency bands. The resonance occurs at the frequency  $f_0$  given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (2.14)$$

where  $L$  corresponds to the inductance and  $C$  corresponds to the capacitance. The resonance bottoms out at the Equivalent Series Resistance (ESR) of the capacitor as discussed in Chapter 1. Another positive peak is observed in Figure 2.16 due to antiresonance between the two parallel decoupling capacitors. The positive peak corresponds to the resonance between the series inductance of one capacitor (ESL) and the capacitance of the other decoupling capacitor. Note that this antiresonance peak is a major issue in PDN design and in the illustrated case leads to the violation of the target impedance. Effect of antiresonance can be mitigated by adding several decoupling capacitors with values distributed in between the two capacitor values considered in this case. The antiresonance peaks become smaller and are smoothed out by the addition of more capacitors. A more effective way to reduce the peaking in the impedance characteristics is to reduce the overall inductance in the PDN [49].

Decoupling capacitance is also added on-chip to control the power supply impedance beyond the frequency range of the bulk capacitors on the board and the package decoupling capacitors. The on-chip decoupling capacitances are added at “hot spots” where a lot of switching activity will likely take place. The decoupling capacitors should be designed such that they do not take up a large amount of area otherwise they will decrease the yield. The on-chip decoupling capacitors reduce the  $di/dt$  noise generated by the on-chip circuitry. To reduce the voltage sag due to many off-chip drivers, decoupling capacitors are also placed on the package and the board.

Also multiple low-inductance power/ground pins are provided for the output buffers to minimize the voltage sag/transient noise in the power distribution network. Immediately after switching, no current flows through the large inductor, and a capacitance divider is established based on the charge conservation law:

$$C_{decap} \cdot V_{cc} = (V_{cc} + \Delta V) \cdot (C_{decap} + C_{sw}) \quad (2.15)$$

$$\Delta V = -\frac{C_{sw}}{C_{decap} + C_{sw}} V_{cc} \quad (2.16)$$

Based on (2.16), to ensure a small voltage fluctuation, the decoupling capacitance  $C_{decap}$  must be much larger than the switching capacitance  $C_{sw}$ .

## **2.4 Chapter Summary**

In section 2.1, FCC's definition of ultra wideband was reviewed. The emission mask for UWB communication, channel modeling techniques, receiver architectures, interference issues as well as multiple access schemes was reviewed.

In section 2.2, history of power line communications was presented as well as channel modeling techniques and noise issues were discussed. Some commercially available power line modems were also presented.

In section 2.3, architecture and design of microprocessor's power distribution network was discussed. Switching noise in the PDN was discussed briefly but will be discussed in more detail in chapter 5. Also, the purpose and design of decoupling solution for a microprocessor PDN was presented.

## **Chapter 3: Feasibility Study Using PDN Models**

PDN models were developed at VTVT and their time and frequency response was studied. High frequency characteristics of the Intel PDN models were analyzed for the existence of pass bands at high frequencies. These two modeling strategies are compared and their point of departures was identified. General non-applicability of the Intel PDN models for high frequency characterization is also described.

### ***3.1 Power Distribution Network Modeling at VTVT***

A detailed power distribution network of a microprocessor is shown in Figure 3.1. The PDN consists of multiple power planes in the package and a branched grid structure on for on-chip power distribution. The structure of the power planes and the on-chip power grid are quite different and hence different modeling strategies are followed for the package and the power grid.

The package consists of multiple plane layers. Depending on the frequency band of interest, the modeling of the planes can be computationally intensive due to their large electrical size at these frequencies. Numerical methods such as Method of Moments (MoM) and Finite Difference Time-Domain (FDTD) have been proposed for analyzing such structures [55]. Although, these are appropriate for arbitrary geometries, more numerically efficient techniques are possible for regular structures. An analytical approach based on solving Maxwell equations was proposed in [56]. The non-linear solution is then converted to a linear solution for constructing Spice models based on resonator principles. The method is numerically efficient and is valid for frequencies in the GHz range. Therefore this approach for chosen for modeling the power planes in the VTVT PDN model and will be discussed in more detail in the following section.

For the on-chip power grid, the influence of inductance grows more significant as frequency increases. Effective methods for inductance extraction in multiconductor structures with dielectrics such as those found in the on-chip power grid are presented

in [57]. Earlier works on high frequency modeling of on-chip interconnects focused mostly on two dimensional transmission line models. The two dimensional transmission line theory requires that the cross-sections of the conductors remains constant for a distance which is long compared to the cross-sectional dimensions. As the structures have become dramatically small with improvements in process technology, the three dimensional aspects become more important. In this area also, modeling work has proceeded using FDTD techniques [58] and integral equation formulations [59]. More recent approaches have concentrated on translating the electromagnetic problem to equivalent circuit models where the complexity of the numerical methods is limited by using many different approximations [58][61]. In the VTVT model equivalent Spice models of electromagnetic wave models are used for modeling the on-chip power distribution network. The modeling and extraction of RLC values are discussed in sections 3.1.2 and 3.1.3.

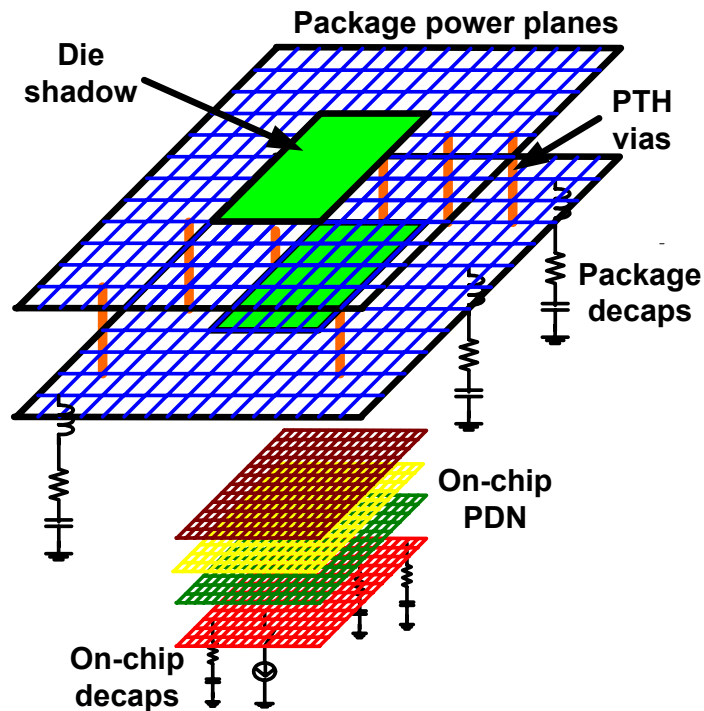


Figure 3.1: Package and on-chip power distribution network of a microprocessor

### 3.1.1 Cavity Resonator Model (CRM) of the Package Power Planes

The most important element of PDN in high-speed packages running over GHz is the power and ground planes. Recent publications show the computational efficiency and accuracy for the modeling and simulations of a planar structure IC package based on the cavity resonators [56]. The CRM considers wave propagation, which is far more accurate for current high-speed VLSI systems. The power-ground plane pairs work as cavity resonators supporting radial waves, which propagate into the space between the plane pairs. At the edge of the planes, the radial waves are reflected and cause resonance in the steady state. This behavior can be represented by computing the impedance characteristics seen by an arbitrary location of ports on the planes. A planar package model was adopted for accuracy and computational efficiency.

Based on [56], for a single plane pair, impedance characteristics can be represented by (3.1), which represents the plane pair as an equivalent circuit formed by using parallel resonant circuits and ideal transformers. The impedance between port  $i$  and port  $j$  is given by

$$Z_{ij}(\omega) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{N_{mni} N_{mnj}}{1/j\omega L_{mn} + j\omega L_{mn} + G_{mn}} \quad (3.1)$$

Where

$$L_{mn} = \frac{d}{\omega_{mn}^2 ab\epsilon},$$

$$C_{mn} = \frac{ab\epsilon}{d},$$

$$G_{mn} = (ab\epsilon/d) \omega_{mn} \left( \tan \delta + \left( \sqrt{2/\omega_{mn}\mu\sigma} \right) / d \right),$$

$$N_{mni} = \epsilon_m \epsilon_n \cos\left(\frac{m\pi x_i}{a}\right) \sin c\left(\frac{m\pi t_{xi}}{2a}\right) \cos\left(\frac{n\pi y_i}{b}\right) \sin c\left(\frac{n\pi t_{yi}}{2b}\right).$$

$L_{mn}$ ,  $C_{mn}$ , and  $G_{mn}$  form a parallel resonator  $R_{mn}$  and the entire SPICE equivalent circuit is shown in Figure 3.2 as in [56]. More details on the modeling of the power planes and the noise levels can be found in [62].

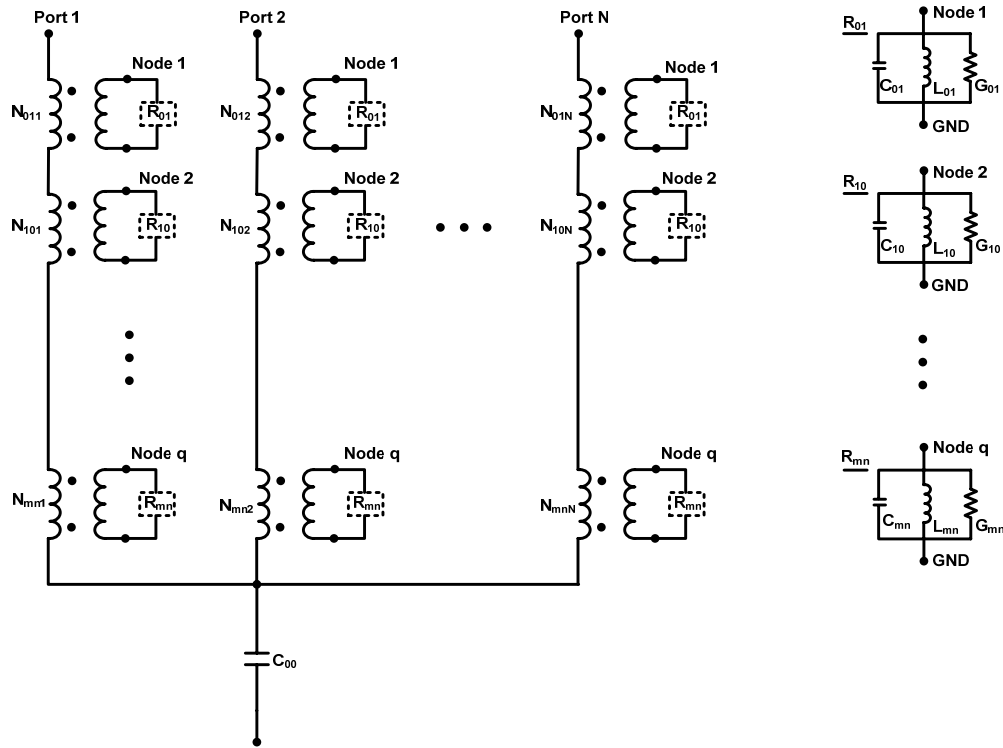


Figure 3.2: Model of the power planes based on CRM

### 3.1.2 On-chip Power Distribution Network

The lumped second order model does not give insight for estimating the desired characteristics of delay and attenuation at several locations on a metal wire. A simple distributed RLC model is appropriate for the investigation of pulse propagation through an on-chip power distribution grid. In the RLC model, the die area is divided into a grid of cells. The power and ground distribution networks within each cell are reduced to a simplified macro model. These macro models form an RLC grid model of an on-chip power distribution network, is shown in Figure 3.3 [63]. Several methods for distributed modeling of the on-chip power grid have been reported [99]-[101]. Systematic procedure for the extraction of the RLC values is discussed in detail in the following section.

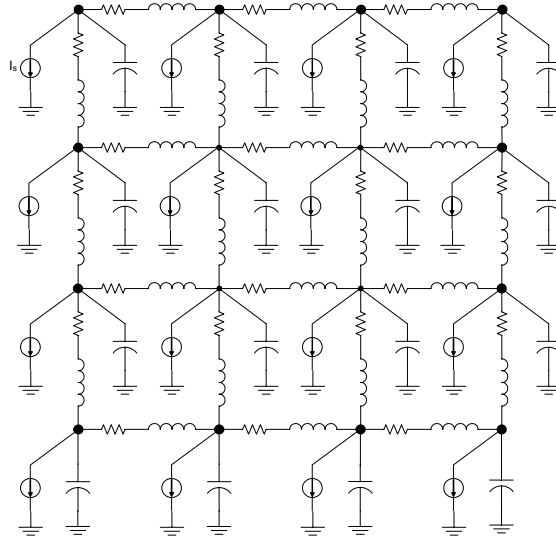


Figure 3.3: A 3-stage  $\Pi$ -type power distribution network model

### 3.1.3 Parasitics Extraction for the On-Chip Power Grid

#### 3.1.3.1 Resistance

The resistive components of metal wires cause voltage drop on the on-chip power grid. The dominant effect is the delay and attenuation from the time constant (which is the product of resistance and capacitance). The estimation of resistance of metal wires is as follows, for a uniform conducting slab whose dimension is  $w$  (width)  $\times l$  (length)  $\times t$  (thickness), the resistance can be estimated as

$$R = \left( \frac{\rho}{t} \right) \cdot \left( \frac{l}{w} \right) \quad (3.2)$$

where  $\rho$  = resistivity

$t$  = thickness

$l$  = conductor length

$w$  = conductor width

The expression in (3.2) can be rewritten as

$$R = R_s \cdot \left( \frac{l}{w} \right) \quad (3.3)$$

where  $R_s$  is the sheet resistance having units of  $\Omega/\text{square}$  [98]. Thus, to obtain the resistance of a metal wire, we only need to know the length, width, and sheet resistance. Typically, the sheet resistance is provided with the process details. The upper metal layers have reduced resistivity and delay, since they are usually thicker. Typically for effective distribution of power and ground, the thicker metal layers have been used, and frequently more than necessary are used. This overestimation results in the waste of a valuable resource (i.e. the upper metal layers) in an integrated circuit. The termination of the metal width depends on the requirement of voltage drop, die size, and the number of power pins.

### 3.1.3.2 Inductance

As technology advances, the integration level and operating frequency of an integrated circuit increases, so the inductive loss of on-chip metal wires cannot be ignored. The inductance of power distribution system can have a significant impact on signal integrity. It is difficult to model the inductance accurately (yet simply) because of non-locality effect and an unknown return path. Inductance of a conductor on the silicon substrate can be obtained from the following equation under the assumption of negligible thickness of the conductor (e.g. a metal wire) and  $w < h$ .

$$L = \frac{\mu}{2\pi} \ln \left( \frac{8h}{w} + \frac{w}{4h} \right) \quad (3.4)$$

where  $\mu$  = permeability,  $h$  = thickness of the substrate and the conductor on it (which can be approximated as the thickness of the substrate due to the large difference in the order of the thickness of a substrate and a conductor), and  $w$  = width of the conductor. Although the thickness of the silicon substrate varies based on the process and manufacturing company, the order of the thickness of a substrate is much greater than that of a conductor. Thus the thickness  $h$  in (3.4) will be approximated as the thickness of the silicon substrate, which ranges from 250  $\mu\text{m}$  to 1000  $\mu\text{m}$ . In the case of package

inductance, manufacturers usually provide values (normally in the range of 3-15 nH for the peripheral I/O type packages and 0.5-2 nH for the array I/O type packages). The inductance of a bond wire is an important consideration for inductive spikes, when a large current is drawn through a wire in a short period of time. Recently, on-chip inductance has also been a focus due to increased chip dimensions (number of devices) and thus, increased chances of the simultaneous switching of the increased number of devices.

### 3.1.3.3 Capacitance

Capacitive parasitics result from the routing conductors on the substrate, and the basic principle is the parallel-plate capacitor model ( $C = \epsilon A/d$ ) where  $A$  is the area of the parallel plate capacitor,  $d$  is the insulator thickness, and  $\epsilon$  is the permittivity of the insulating material between the plates. However, the parallel-plate capacitor model ignores the fringe effect at the edges of the conductor due to its finite thickness. The fringing field increases the effective area beyond that of the parallel plates of the adjacent conductors. Due to the computational complexity for finding the capacitances of many conductors, many research activities have explored approximations to this calculation. An empirical formula that is computationally efficient with reasonable accuracy is provided by [64]

$$C = \epsilon \left[ \left( \frac{w}{h} \right) + 0.77 + 1.06 \left( \frac{w}{h} \right)^{0.25} + 1.06 \left( \frac{t}{h} \right)^{0.5} \right] \quad (3.5)$$

where  $\epsilon$  is the permittivity,  $w$  is the width,  $h$  is the height, and  $t$  is the thickness of the geometry of a conductor of interest. For multiple conductors' capacitance, one research study shows the general tendency of typical conductor capacitance as a function of spacing and width. As the spacing increases, the capacitance decreases; as the width increases, the capacitance increases [65]. Other approaches to capacitance modeling may be referred to [66]-[68].

### 3.1.4 Time Domain Simulation of the VTVT PDN Model

Time domain simulations of the PDN model were carried out. A Gaussian input pulse was applied at the power pin on the package and the output is observed at an internal node on the on-chip power grid. The input and output pulses without the noise added are shown in Figure 3.4.

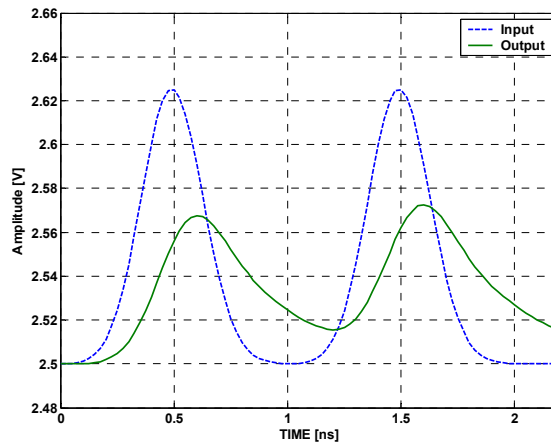


Figure 3.4: Output pulse on the on-chip power grid o

In Figure 3.4, it can be seen that the output pulse is a distorted version of the input pulse. Due to idealities in modeling, the multipath effects are ignored, and the output pulse merely appears as a delayed version of the input pulse and slightly distorted version of the input pulse. As a next step, thermal noise is added to the simulation and the time domain simulation results are shown Figure 3.5. The switching noise in the PDN is quite complex and can only be modeled by statistical means. The characteristics of the PDN noise, measurement and modeling techniques will be described in more detail in chapter 5 of this dissertation. With the addition of thermal noise, the output pulse is a distorted version of the input pulse.

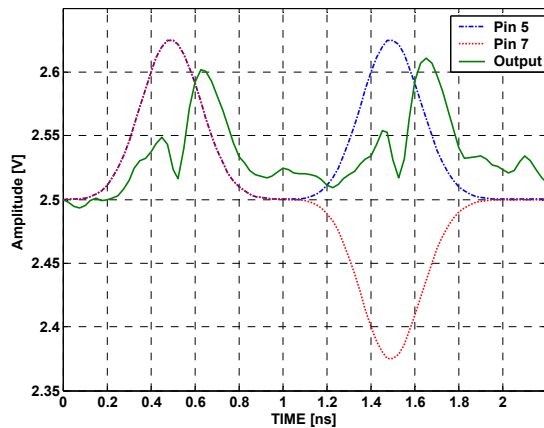


Figure 3.5: Output pulse on the on-chip power grid (with noise added)

### 3.1.5 Frequency Response

The frequency response of the Virginia Tech PDN model is shown in Figure 3.6. The y-axis is labeled as a percentage of  $V_{out}/V_{in}$  i.e. output voltage observed at an internal node expressed as percentage of the input signal. Therefore Figure 3.6 shows the transfer characteristics of the PDN as a function of frequency up to 6 GHz. Distinct pass bands are observed in the high frequency transfer characteristics of the PDN. Specifically for the processor whose package was modeled (IBM PowerPC 750), pass bands are observed at 1.8 GHz, 3 GHz and at 4.6 GHz where about 40%, 25% and 25% of the input signal passes through the PDN. These pass bands can be used for communication through the power distribution network using I-UWB signaling as proposed previously.

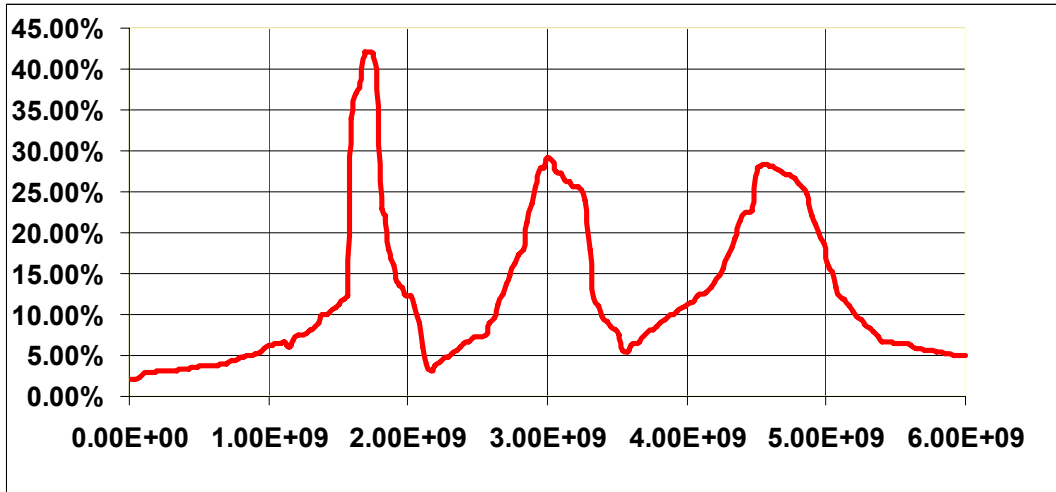


Figure 3.6: Frequency response of the VTVT PDN model

## 3.2 Intel PDN Model

### 3.2.1 Lumped Model of the Power Distribution Network

Figure 3.7 shows the lumped model of a microprocessor's power distribution network [49]. The overall power distribution system consists of a hierarchical structure, which spans the voltage regulator, printed circuit board, packages, and integrated circuits. The overall characteristics of the power distribution networks of the power distribution system depend on the operating frequency range. The parasitics of the power (ground) plane include resistance and inductance. As the number of planes increases, the parasitics of resistance and inductance decrease because of the shunt connections among planes. The other parasitics include the equivalent series resistance (ESR;  $R_y^c$ ), the equivalent series inductance (ESL;  $L_y^c$ ), and the capacitance ( $C$ ;  $C_y$ ) of the decoupling capacitors between power and ground lines. Figure 3.7 shows the lumped circuit model equivalent of the power distribution network. The subscripts  $r$ ,  $b$ ,  $p$ , and  $c$  denote regulator, board, package, and chip respectively. The superscript  $p$ ,  $g$ , and  $c$  denote the power, ground and decoupling capacitors. The power and ground planes have parasitics of resistance and inductance of  $R_x^{p(g)}$  and  $L_x^{p(g)}$ , respectively. The

superscript  $p(g)$  denotes the power (ground) plane and subscript  $x$  represents  $r$ ,  $b$ ,  $p$ , and  $c$ . The ESR, ESL, and C in decoupling capacitors can be represented by  $R_y^c$ ,  $L_y^c$ , and  $C_y$ , respectively. The superscript  $c$  denotes decoupling capacitors and the superscript  $y$  represents  $b$ ,  $p$ , or  $c$ .

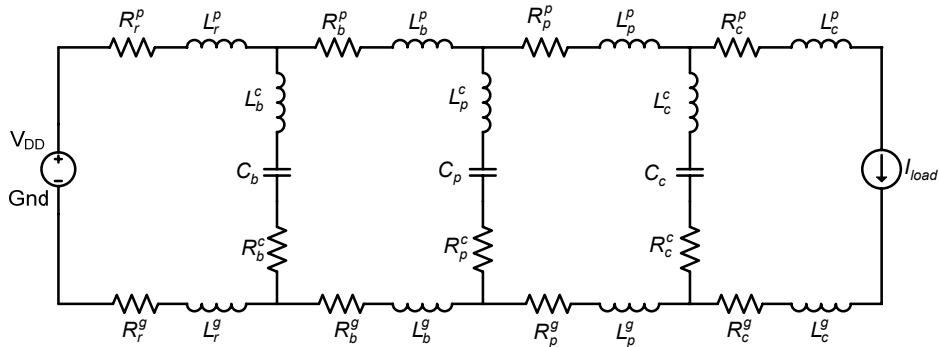


Figure 3.7: Lumped model of the microprocessor power distribution network

### 3.2.2 Package Model at Intel

Although the package models developed at Intel are based on lumped equivalent model, they are extremely well detailed. The package layers are modeled using 3D modeling and all the different features are accurately modeled by incorporating integrated capacitor-via-planes and detailed models of different levels of interconnect components, i.e. capacitor to micro-via, micro-via to planes, and capacitor planes. Noisy spots on the processor are located through initial simulations and package capacitors are placed close to these noisy spots. The model also includes the position and model of the package decoupling capacitors.

Two different approaches are used for developing the 3D model of the power distribution network [69] [49]. In the first method, a 3D model is developed directly from a one-dimensional lumped model. It divides the package and motherboard into small tiles and extract the parasitic for these tiles with field solver in  $x$ ,  $y$ , and  $z$  directions. These parasitics can then be used in Spice like simulators. The main advantage of this method is that it could be integrated with virtually any transistor level

circuit simulator. In the second method, a time domain field solver like SPEED2000 is utilized. These solvers are generally limited in their ability to model a wide variety of circuits but are very good in capturing wave effects and modeling three dimensional structures. The circuits are then combined with a three-dimensional package-motherboard model in SPEED2000 as shown in Figure 3.8. The small rectangular planes at the top represent the package power planes and the mother board is represented by the larger planes at the bottom. The yellow dots represent the socket pins on the motherboard. On the top layer of the package, there are vias representing C4 bumps and are connected to the two-dimensional die pad ring model (not shown).

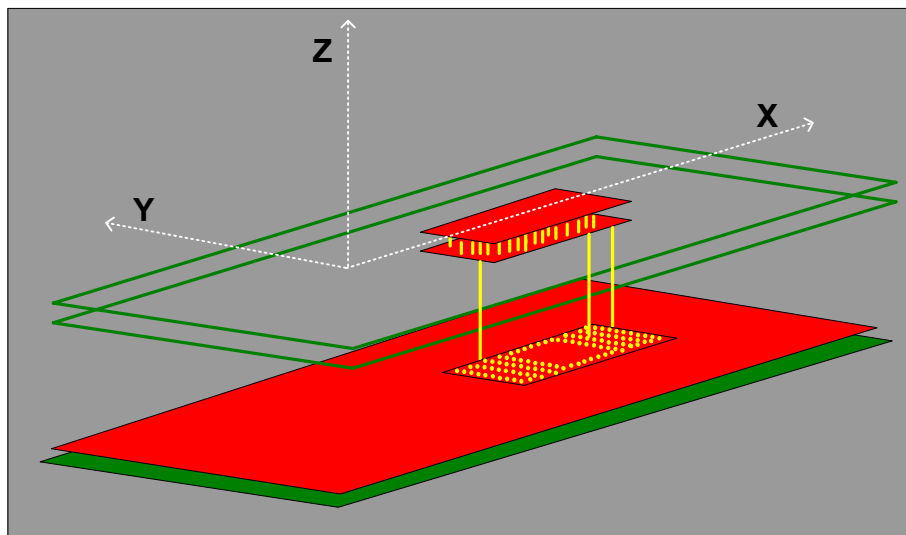


Figure 3.8: Package modeling at Intel

### 3.2.3 On-Chip Power Grid Model

The on-chip power grid model is shown in Figure 3.9. Again the metal grid is divided into a square grid and modeled as a series resistance, inductance with a capacitance to ground where R, L, C values are estimated using process specific parameters.

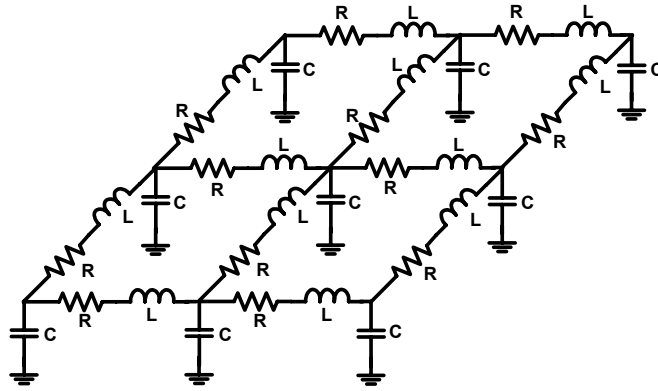


Figure 3.9: On-Chip power grid model at Intel

### 3.2.4 Frequency Response

The frequency response of the PDN model studied at Intel is shown in Figure 3.10. Similar to Figure 3.6, here also the y-axis is the ratio of  $V_{out}/V_{in}$  expressed as a percentage. Lumped modeling of the PDN model does not model the high frequency characteristics of the PDN adequately and consequently no pass bands are observed in the transfer characteristics. The whole PDN looks like a low pass filter and the loss through the PDN increases monotonically at frequencies beyond a few hundred KHz except for a peak between 100 and 200 MHz. This corresponds to the resonance in the lumped model of the power plane inductance and capacitance.

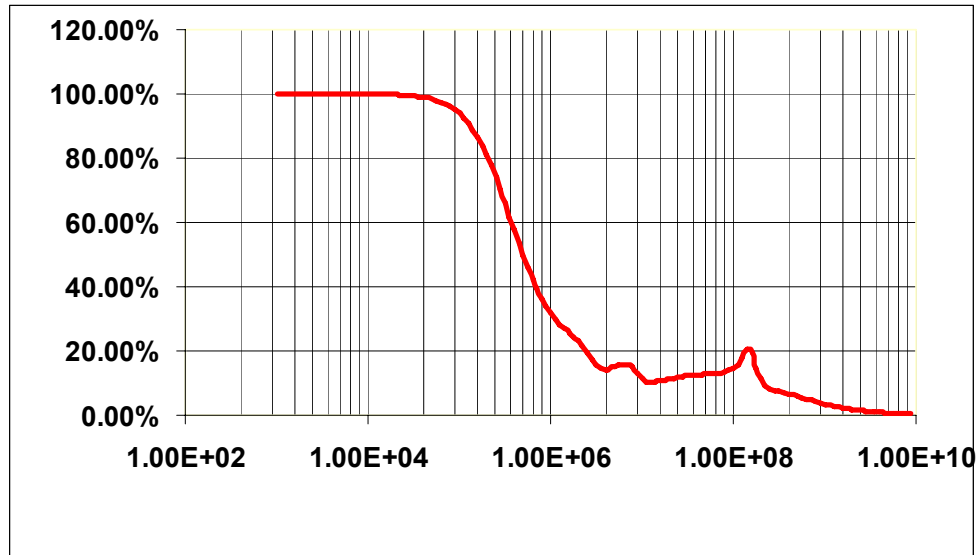


Figure 3.10: Frequency response of the PDN model developed at Intel

### 3.3 Comparison of Intel and VTVT PDN Models

At this point of feasibility study using PDN models, the frequency response of the PDN models developed at VTVT and the PDN models studied at Intel point in two different directions.

The VTVT PDN model was based on the cavity resonator model that captures the frequency dependence of R, L, C components using transformers with lossy tank circuits in the secondary of the transformers. Pass bands exist between clusters of the resonant frequencies of the different tank circuits depending on the propagation modes of the high frequency waves. Referring back to Figure 3.6, distinct pass bands were observed in the frequency range from GHz to 3 GHz.

The PDN models studied at Intel were mostly based on lumped modeling which are not valid beyond 500 MHz. Current Power Delivery Intel SPICE models are valid admittedly valid only up to ~ 200 MHz. Full wave electromagnetic models capture the frequency dependent variation of the R, L, C elements in the PDN power planes. These

variations are not captured in the Intel PDN model and consequently, the loss through the PDN increases continuously beyond 200 MHz.

Based on the conclusions of the feasibility study using PDN models, we concluded that the most direct way to prove the proposed communication method is to use direct high frequency measurements through the PDN of the microprocessors.

### **3.4 Chapter Summary**

In section 3.1, the PDN modeling at VTVT was described in detail. The power planes in the package was modeled using cavity resonator models, and detailed extraction of the on-chip power grid was performed using process data, empirical modeling and IBM PowerPC power grid details.

In section 3.2, PDN models studied at Intel was presented. The emphasis in Intel models was the exact 3D modeling of the complex flip-chip packaging structure rather than accurate high frequency modeling. The overall frequency response behaved like a low pass filter with no pass bands at high frequencies.

In section 3.3, the basic elements of high frequency PDN modeling is described and the difference between the two modeling techniques is explained. Although, accurate high frequency modeling of proprietary Intel PDN design would be valuable due to scaling trades and significant changes from one generation of processor to the next, accurate high frequency modeling can be time consuming. Therefore we concluded that PDN characterization using high frequency measurements was decidedly more appropriate and a direct way to study the feasibility of the proposed communication method.

## **Chapter 4: Feasibility Study through High Frequency Measurements on the PDN**

In this chapter, the feasibility study conducted through direct high frequency measurements is described. Measurements were conducted on the PDN of both passive and active dies of the 65nm Pentium 4 PDN and the 45 nm Core 2 Duo processors. Measurements were also taken at different locations and on multiple samples of the same die to estimate the effect of spatial variations and process variations on the transfer characteristics of the PDN. Narrow, sporadic and migratory pass bands were identified on the transfer characteristics of the Pentium and Core 2 Duo processor's PDN.

### ***4.1 Measurements on the PDN of a Cold Microprocessor Die***

In this section, setup for measuring the transfer characteristics of the PDN on a cold microprocessor die is described. Measurement results from a 65 nm Pentium 4 PDN and the 45 nm Core 2 Duo PDN are presented. Spatial and intra-die variations of the PDN transfer characteristics are also presented. Finally, the significant findings are summarized.

#### **4.1.1 Measurement Setup**

The PDN channel was characterized in the frequency domain using measurements with a network analyzer. Wireless channels have been characterized for UWB communication using frequency domain measurements [70][71][72] or using time domain measurements [73][74] and both the methods have been shown to be equivalent with a few caveats [75]. Appropriate fixtures required to connect the network analyzer to the PDN were not readily available due to the unique nature of our

research proposal. We were able to piggy back on a measurement setup typically used for power supply noise measurements and modify it to suit our needs.

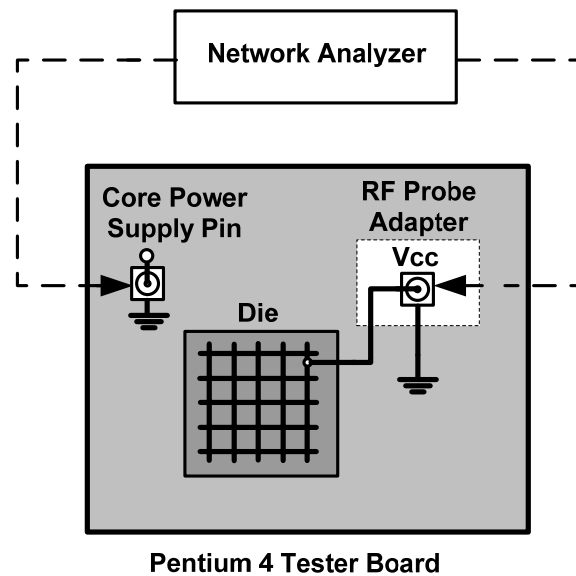


Figure 4.1: Measurement setup schematic

The measurement setup is shown in Figure 4.1. The processor is mounted on a tester board. One port of the network analyzer was connected to a core power supply pin on the tester board and the other port of the network analyzer was connected to a node on the on-chip power distribution network. This setup ensures that the complete microprocessor power distribution network is characterized by the measurements, including the power planes in the tester board, package power planes, on-chip power grid and all the different decoupling capacitors. A launcher needle used in Time Domain Reflectometer (TDR) measurements to characterize tester board power planes was used to connect one port of the network analyzer to the tester board's core power supply pin.

A probing node on the on-chip power grid was created through the back of the microprocessor die using electropolishing, chemical etching and metal deposition using focused ion beam (FIB). Since the current and future generation of microprocessor flip chip packages are aimed at increasing the pin count to area ratio, internal nodes are

accessible for monitoring/post-silicon debugging only through the back of the die through the substrate. *Electropolishing* is typically used to thin the substrate and chemical etching is used to create a stepped ladder like structure to gradually expose the internal node in the die. Finally, Focused Ion Beam (FIB) is used to deposit additional metal over the internal Vcc node via *ion beam induced deposition* [77] to be visible under the microscope and for making better contact using picoprobes [76]. A picoprobe, connected to the second port of the network analyzer was used to make contact with the exposed Vcc node. Since the probing node is created through the back of the die, the metal layers are seen in the increasing order (i.e. first M1, then M2 and so on) and therefore the lowest metal layer used on the on-chip power grid (i.e. M2) is conveniently exposed first. In this way, the picoprobe makes direct contact to the location where the transmitter/receive block would be eventually located and the PDN is completely characterized through measurement including the several metal layers in the on-chip power grid.

#### **4.1.2 Measurements on 65 nm Pentium Die**

For measurements on a cold die, measurements were taken with the processor mounted on the tester board. A network analyzer was used to measure the transfer characteristics of the PDN. The measured scattering parameters (S-parameters) using the network analyzer are expressed as the voltage ratio  $|V_{out}/V_{in}|$  (in percentage) for readability. The transfer characteristics measured on a single sample of a cold 65nm Pentium processor's PDN is shown in Figure 4.2. The transfer characteristics show the existence of narrow sporadic pass bands above 200 MHz. The largest pass band and peak propagation is observed around 2 GHz over a 200 MHz band. As expected, the PDN is quite lossy with only about 5~7% of the signal passing through the PDN in narrow sporadic bands.

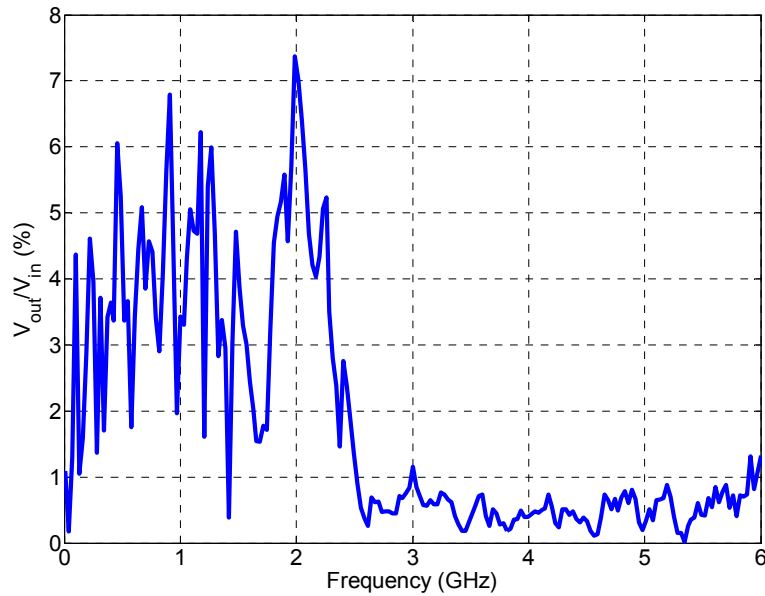


Figure 4.2: Transfer characteristics of the cold 65 nm Pentium PDN

#### 4.1.3 Measurements on Cold 45 nm Core 2 Duo Processor Die

Unlike the 65 nm Pentium 4 die, the transfer characteristics were measured on few samples of the cold 45 nm Core 2 Duo processor's PDN at different locations. The spatial and intra-die variations of the transfer characteristics measured on different Core 2 Duo samples are discussed in the next section. The *averaged* transfer characteristics are shown in Figure 4.3. The transfer characteristics of the Core 2 Duo PDN also show narrow sporadic passbands beyond 200 MHz where about 5~7% of the input signal passes through the PDN. The most noticeable passbands are observed around 500 MHz, 850 MHz and 1.1 GHz in bands much narrower than the ones observed on the 65 nm Pentium 4 PDN.

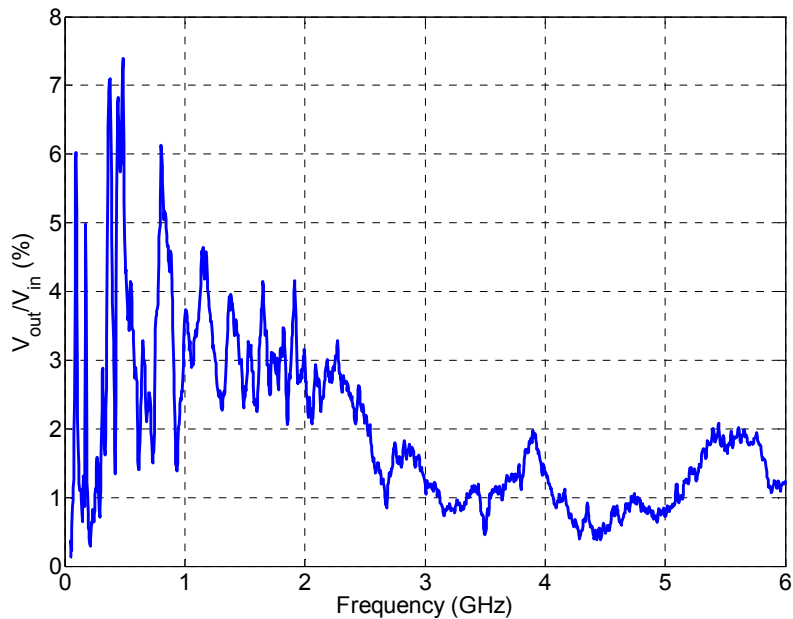


Figure 4.3: Transfer Characteristics of the cold 45nm Core 2 Duo PDN

There is a very little correlation between the transfer characteristics measured on the 65nm Pentium PDN and the 45nm Core 2 Duo PDN. Further, the large passband observed around 2GHz on the 65nm Core 2 Duo PDN is not seen in the transfer characteristics of the 45nm Core 2 Duo PDN. Expectedly, the passbands move from one generation of processor to the next because of the difference in the package power plane design, on-chip power grid design as well as the difference in the dimensions of the metal layers in different process technologies.

#### 4.1.3.1 Spatial and Intra-die Variations

Measurements were carried out on 3 different samples of the 45nm Core 2 Duo processors and two randomly picked locations on the core Vcc. On one sample, one exposed node on the on-chip power grid was damaged during measurements and therefore only five different transfer characteristics were measured. The five individual measurements and the superimposed average are shown in Figure 4.4. Across different

parts and different locations, the transfer characteristics essentially remain the same with minor differences. Therefore, irrespective of the location of the internal node, the transfer characteristics seen between the controller chip (discussed in application scenarios in section 1.4) and the internal transmitter/receivers would essentially be similar.

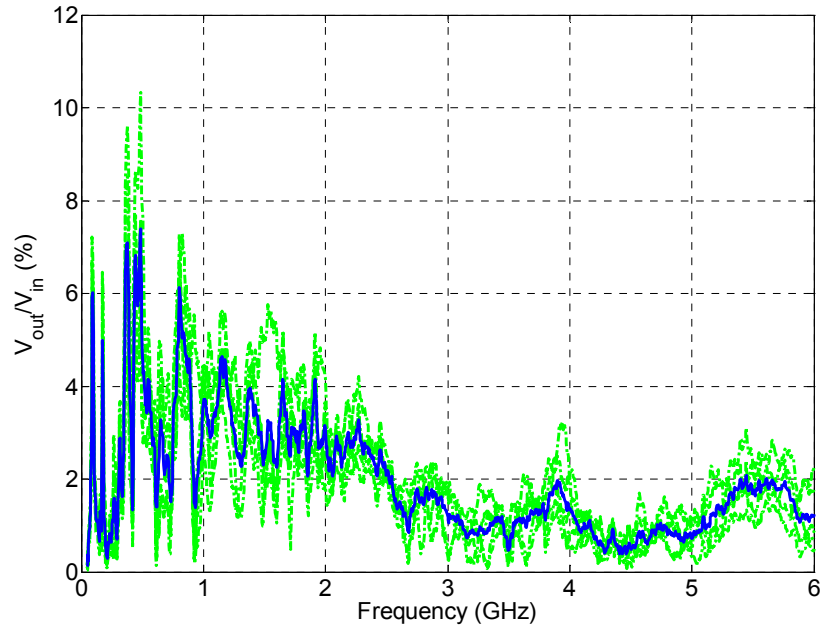


Figure 4.4: Spatial and intra-die variation of the transfer characteristics in 45 nm Core 2 Duo (Individual transfer characteristics are shown in light shade and the average shown in a dark shade)

#### 4.1.4 Significant Findings

From measurements, we can observe that the pass bands do exist in the high frequency transfer characteristics of the PDN. The passbands observed are narrow and sporadic. For the 65 nm Core 2 Duo, the pass bands are observed at 900 MHz, 1.1 GHz and the biggest pass band is observed at 2 GHz. From the transfer characteristics of the 45 nm Core 2 Duo PDN, pass bands are observed at 500 MHz and at 850 MHz. Although narrow pass bands are observed, the pass bands move from one generation of

processors to the next. Instead of identifying a single pass band for communication over the PDN, the more viable method would be cover the entire pass band of interest with a pulse shape with a relatively wide spectrum (say from 400 MHz to 3 GHz). Note that no pass bands were observed beyond 3 GHz.

## 4.2 Measurements on the PDN of Active Core 2 Duo Die

In this section, the measurement setup for the active processor is discussed and the measured transfer characteristics of the PDN are presented. The influence of temperature on the transfer characteristics is discussed based on observations. Further, the transfer characteristics measured on the PDN of active and cold processor dies are compared and the significant findings from this measurement campaign are summarized.

### 4.2.1 Measurement Setup for an Active processor

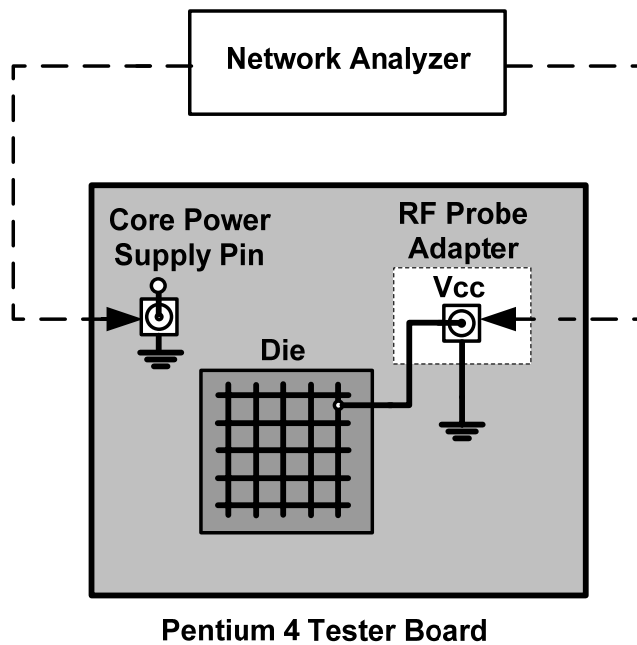


Figure 4.5: Measurement setup schematic

The measurement setup for measurements on an active processor is shown in Figure 4.5. This setup is quite similar to the one used for measuring the transfer characteristics of the cold microprocessor shown in Figure 4.1. The processor is mounted on a tester board. One port of the network analyzer was connected to a core power supply pin on the tester board and the other port of the network analyzer was connected to a node on the on-chip power distribution network. This setup ensures that the complete microprocessor power distribution network is characterized by the measurements, including the power planes in the tester board, package power planes, on-chip power grid and all the different decoupling capacitors. A launcher needle used in Time Domain Reflectometer (TDR) measurements to characterize tester board power planes was used to connect one port of the network analyzer to the tester board's core power supply pin. A probing node was created using Focused Ion Beam (FIB) to expose a node on the on-chip power grid. A RF probe connected to the second port of the network analyzer was used to make contact with the exposed Vcc node. Since the microprocessors are in a flip-chip package, the probing node created through the back of the die exposes the second level metal layer (M2) in the on-chip power grid, thereby characterizing the PDN channel up to a location where the transmitter/receive block would be eventually located.

For active measurements, the board was mounted on a production-level tester and test loop was continuously run on the processor. Since access to the production-level testers for research projects is limited, only few measurements were possible on the active microprocessor. Also, when the processor is active and running at full load, external thermal cooling is applied by pumping cool air which precludes access to the exposed node on the on-chip Vcc through the back of the die. Therefore during active measurements, the processor was run at the lowest core Vcc voltage and the clock frequency at which the processor was functional. Consequently, temperature effects are minimal even when the processor was let to run for an extended period of time, because the heat generated is much lesser than what would be generated in a processor running a normal or nearly full load. The temperature effects would be discussed in more detail in section 4.2.3. The only difference between the setup shown in Figure 4.1 and the one shown in Figure 4.5 is that external DC blocks (not shown in the figure) are required in

active processor measurements to protect the Network analyzer because the input ports are designed to measure only AC voltages.

#### 4.2.2 Measurements on Active 45 nm Core 2 Duo

As mention in the previous section, the processor was run at the lowest functional core Vcc voltage and clock frequency. At this settings, the processor was drawing an average current  $< 7A$ . Based on discussions with thermal cooling experts at Intel, normal ambient air-circulation was deemed sufficient for thermal reliability at these current levels.

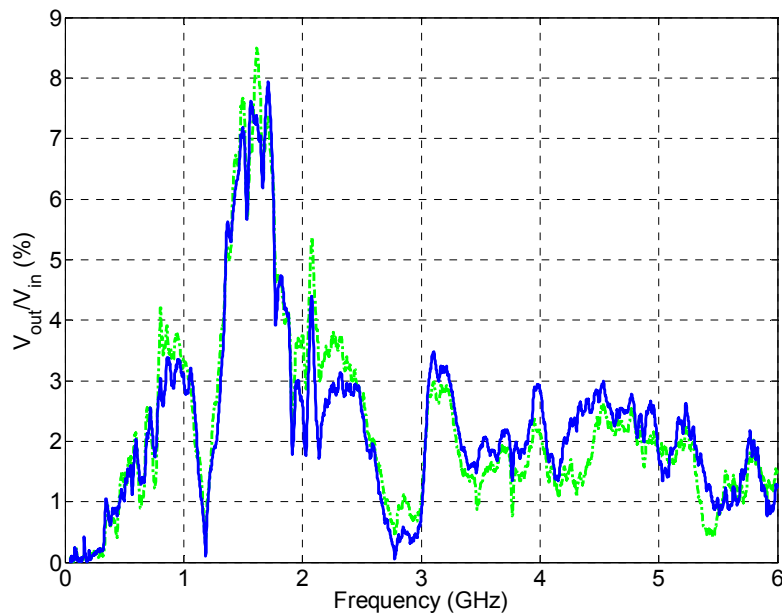


Figure 4.6: Transfer Characteristics on a powered up vs. powered down Core 2 Duo processor (dark shade corresponds to powered up processor, light shade corresponds powered down processor)

The transfer characteristics were measured with the 45 nm Core 2 Duo processor mounted on the production-level tester under powered down as well as well as powered-up conditions. The measured transfer characteristics are shown in Figure

4.6. Again only 5~7% of the input signal passed through the PDN and the difference between the transfer characteristics on the powered up and the powered down processors are minimal. However, the transfer characteristics look smoother and quite different from the transfer characteristics measured on the cold Core 2 Duo processors, shown in Figure 4.4. Recall that the measurements on the cold Core 2 Duo processor were taken when the tester board was not mounted on the tester. The extra capacitance and inductance associated with the tester has moved the pass bands. In this case, one large pass band is observed around 1.4 GHz with about a 500 MHz bandwidth and hardly any sporadic pass bands are observed.

### **4.2.3 Temperature Effects**

During typical operating conditions, significant heating takes place in the die and the effect of temperature on the measured transfer characteristics is an important concern. To study the temperature effects, the part was allowed to run for an extended period of time (~30 minutes) and the transfer characteristics were measured again. No noticeable difference was observed between the measurements at different time instances. Since the part was drawing only a small percentage of the full-load current, it could be argued that the part wouldn't have heated up significantly. However, we may conclude that small variations in temperature do not have an appreciable effect on the measured transfer characteristics.

### **4.2.4 Comparison of Active and Passive Dies**

The major objective of this exercise is to compare the transfer characteristics on the PDN of cold and active dies. Figure 4.6, helps us compare the difference in the transfer characteristics of the passive vs. active die. As can be seen, the transfer characteristics of the PDN in an active and a cold microprocessor die are essentially the same, with very minor differences. This leads to the important conclusion that, as long as the final setup is established, the transfer characteristics of the active die is

essentially the same as one on the passive die. More importantly, the result in Figure 4.6 helps to prove that the proposed method is applicable in active microprocessor dies as well, which leads to a broader applicability of the method as was originally envisioned.

#### **4.2.5 Significant Findings**

From the pass band measurements, it can be seen that the transfer characteristics are very much dependent on the setup inductances and capacitances i.e. whether the part is mounted on the tester board, on the tester or on the mother board. However, since the pass bands move from one generation of processor to the next as well as depending on the setup, we can conclude that the pulses used for communication should cover entire spectrum of sporadic and the occasional wide pass bands observed across different processors and setups. The pulses should have  $\sim 2$ GHz bandwidth, covering the frequency range 300 MHz to about 2.5 GHz. According to one expert at Intel, pulse amplitude of 50 mV and a period of 100ps were suggested as an acceptable level and duration to cause minimal interference to the processor operation. Conclusions derived based on significant findings as well as suggestions by Intel experts are considered in a system level study discussed in section 5.3.

### **4.3 Chapter Summary**

In section 4.1, measurements results from the PDN of a cold microprocessor die is presented. The measurement setup was discussed in detail. Measurements were taken on several samples and at different locations to measure spatial and intra-die variations. Finally significant outcomes and inferences from the measurements are presented.

In section 4.2, measurement setup for measuring high frequency characteristics of an active die is described. The PDN transfer characteristics measured on an active 45 nm Core 2 Duo were presented. Comparing the different measurements, we concluded

that the transfer characteristics were very much dependent on the setup used. Pass bands were observed at very high frequencies on every setup showing the viability of the proposed method. Since the bands are moving from one generation of the processors to the next, we concluded that it might be better to cover the entire band of interest with appropriate pulse shapes rather than trying to identify a pass band suitable for communication because such common pass bands do not exist across different generation of processors.

## **Chapter 5: Channel Modeling, PDN Noise and System Design Considerations**

In this chapter, a channel model is developed based on the high frequency measurements conducted on the PDN along the lines of indoor UWB channel models for wireless communications [112]-[114]. Impulse response of the channel is developed based on the S-parameter measurements. Noise measurements were also carried out on the Intel processors to estimate the noise in the channel. The measurement results are presented here. Based on the channel model and the noise measurements a link budget of the communication system is developed. The link budget will be used as the basis for design of transmitter and receiver circuits. Finally some of the system level issues like modulation techniques and the impact of interference caused by the proposed communication method are discussed.

### ***5.1 Channel Modeling***

#### **5.1.1 65nm Pentium Processor PDN**

##### **5.1.1.1 Channel Path Loss and Phase Response**

S-parameters were measured as part of the feasibility study described in previous chapter. The transmission S-parameter ( $S_{21}$ ) represents the transfer function of the channel. The path loss of the 65 nm Pentium PDN communication channel is represented by the magnitude of  $S_{21}$  and the phase of  $S_{21}$  represents the phase response of the channel. The inverse Fourier transform of the complex  $S_{21}$  represents the impulse response of the communication channel. The path loss is shown in Figure 5.1 and the phase response of the PDN channel is shown in Figure 5.2. The path loss measurements show the existence of narrow sporadic pass bands above 200 MHz. The largest pass band and peak propagation is observed around 2 GHz over a 200 MHz band.

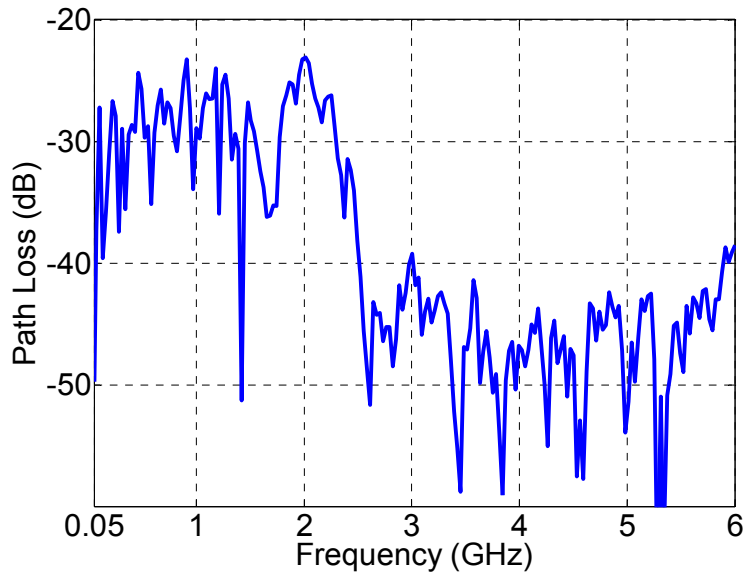


Figure 5.1: Measured path loss of the 65nm Pentium PDN channel

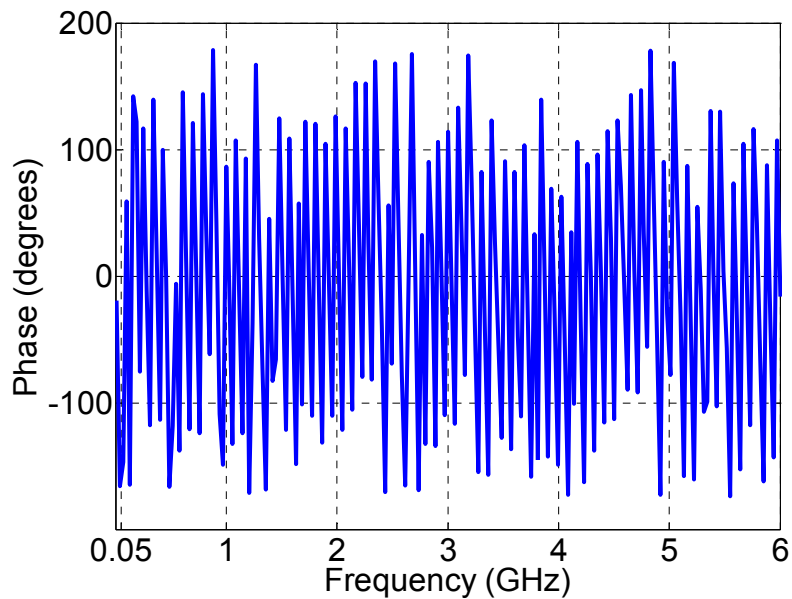


Figure 5.2: Measured phase response of the 65 nm Pentium PDN channel

As expected, the PDN is quite lossy but the peak observed path loss of ~25 dB. The path loss increases above 40 dB beyond 2.5 GHz. The phase of the channel

appears mostly linear except for some phase jumps at frequencies 1.3 GHz, 2.6 GHz and 3.4 GHz. These frequencies correspond to the deep nulls on the path loss characteristics.

### 5.1.1.2 Impulse Response of the Channel

The impulse response of the PDN channel is shown in Figure 5.3 [78]. The impulse response has been normalized and plotted in dB scale. The initial delay of  $\sim 10$  ns is a result of the channel propagation delay between the location of the input and the observation point (i.e. the two port locations of the network analyzer used for measurement of S-parameters). Several multipath components are observed after the arrival of the original pulse. The time resolution is fixed by the range of frequencies swept by the network analyzer (50 MHz to 6 GHz, in our case) and the number of time samples depends on the number of points used in the calibration (201, in our case). The total period of the impulse response is 33.78 ns ( $201 / (6 - 0.05) \times 10^{-9}$ s). An interesting aside is that the second arrival is slightly stronger than the first arrival.

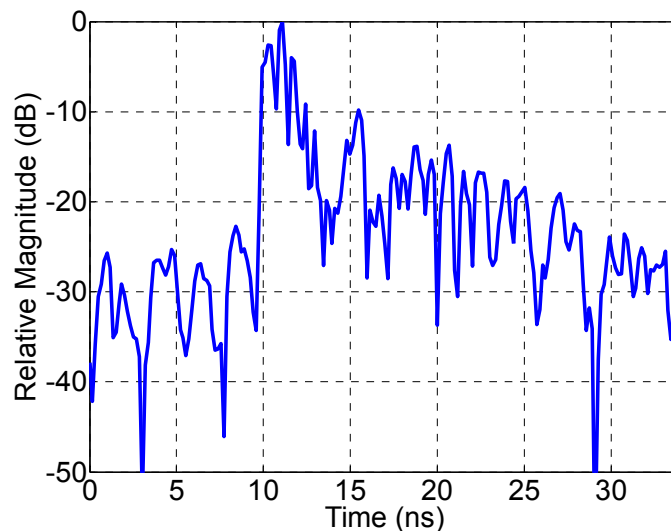


Figure 5.3: Impulse response of the 65 nm Pentium PDN channel

## 5.1.2 45 nm Core 2 Duo Processor PDN

### 5.1.2.1 Channel Path Loss and Phase Response

The path loss of the Core 2 Duo PDN channel is shown in Figure 5.4 and the phase response of the PDN channel is shown in Figure 5.5. The path loss measurements show the existence of narrow sporadic pass bands above 200 MHz. As expected, the PDN is quite lossy but the peak observed path loss of  $\sim 21$  dB is encouraging. The peak propagation is observed around 450 MHz and several narrow sporadic passbands are observed around 800 MHz, 1.2 GHz, 1.4 GHz, 1.8 GHz and at 2.2 GHz with pass loss averaging around  $\sim 27$  dB. The path loss increases continuously above 30 dB beyond 2.5 GHz.

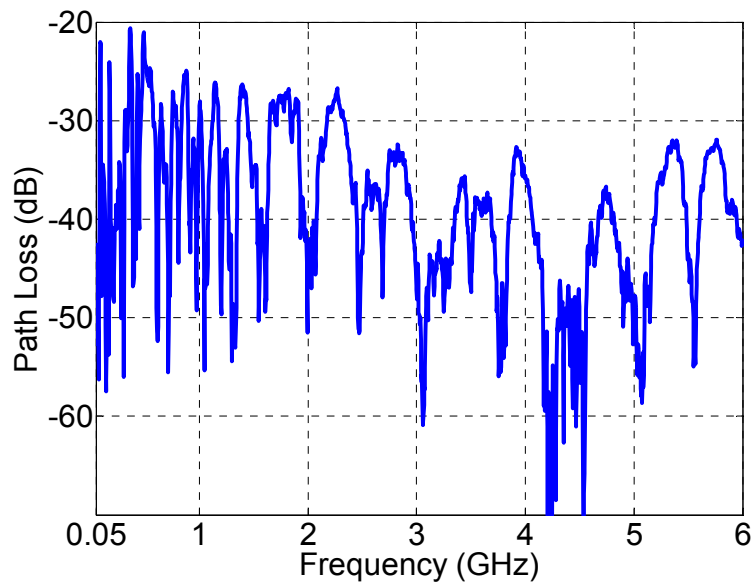


Figure 5.4: Measured path loss of the 45 nm Core 2 Duo PDN channel

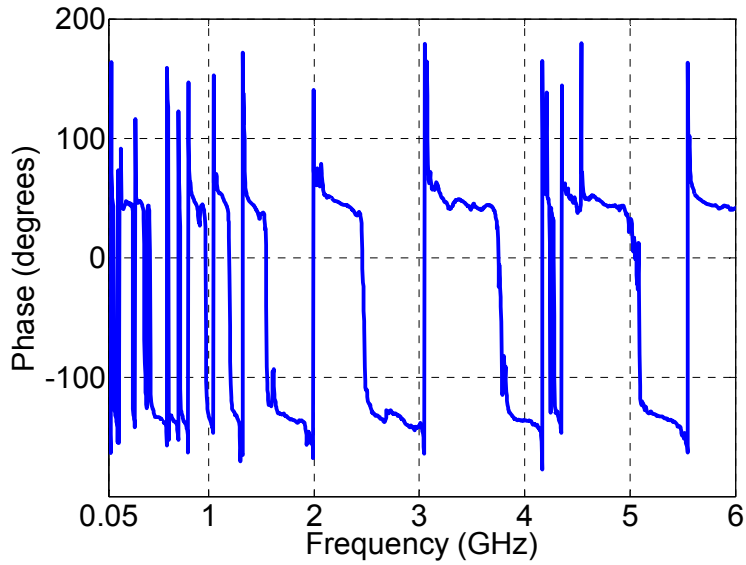


Figure 5.5: Measured phase response of the 45 nm Core 2 Duo PDN channel

### 5.1.2.2 Impulse Response of the Channel

The low pass impulse response of the 45nm Core 2 Duo PDN channel is shown in Figure 5.6. The impulse response has been normalized and plotted in dB scale. The initial delay in this case is much smaller than the one shown in Figure 5.3. Several multipath components are observed after the arrival of the original pulse. The time resolution is fixed by the range of frequencies swept by the network analyzer (50 MHz to 6 GHz, in our case) and the number of time samples depends on the number of points used in the calibration (201, in our case). The total period of the impulse response is 33.78 ns ( $201 / (6 - 0.05) \times 10^{-9}$  s). In this case, the first arrival is the strongest one.

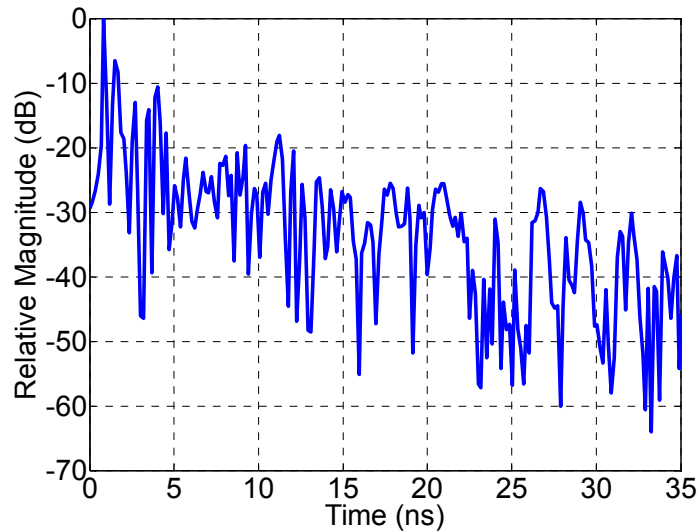


Figure 5.6: Impulse response of the 45 nm Core 2 Duo PDN channel

## 5.2 Noise in the PDN

In this section, the PDN noise characteristics and different techniques for the measurement of on-chip PDN noise are reviewed. A simple model of the PDN noise based on measurements and some of the previously proposed approaches are described. A technique for direct measurement of PDN noise was studied and the setup for PDN noise measurement is described. Measurements on a 65nm Itanium processor and a 45 nm Core 2 Duo processor are presented. The Power Spectral Density (PSD) of the noise measurements is analyzed to estimate the noise level in the PDN channel.

### 5.2.1 PDN Noise Characteristics

Noise in the microprocessor PDN can be broadly classified into three major components [52] [104]-[107].

- Cyclostationary background noise resulting from significant amount of switching synchronous to the main clock.

- Strong deterministic components at the frequency corresponding to the main clock and at the frequency of reference clock input to the PLL.
- Low frequency (20 – 100 MHz) noise resulting from resonances in the impedance characteristics of the PDN.

Due to the enormous number of noise sources in a microprocessor, the background noise tends to a Gaussian process by the central limit theorem. Also, since the majority of switching is periodic with respect to the main clock, the noise can be considered to be cyclostationary Gaussian noise. Incidentally, cyclostationary noise is also observed conventional PLC [80][81].

Interference from internal clocks is deterministic and can be removed by filtering/spreading. Since the spectrum of the pulses are located a higher frequencies, impulse based communications is fairly immune to low frequency noise from PDN impedance resonances so it is not included in the model. Therefore the main concern for the PDN communications is the background switching noise which extends over a bandwidth as wide as 10 GHz [79].

## **5.2.2 PDN Noise Analysis and Measurement Techniques – A Review**

Several PDN noise measurement techniques have been proposed in the literature. Accurate measurement of PDN noise requires on-chip noise measurement because the high frequency noise attenuates very quickly from the location of its origin due to the on-chip, package and board decoupling capacitors. Some of recently reported techniques are reported below,

In [79] the PDN noise is treated as a random process with cyclostationary properties and on-chip VCO and counter was used as an ADC to estimate the statistical properties such as autocorrelation and using it to calculate the Power Spectral Density (PSD) of the PDN noise. The statistical variations of the random noise can be estimated from the measurement data. The PDN noise on an Itanium processor was measured using this technique and the results are reported in [52]. With a core supply voltage of 1.05V, sampled noise voltage is observed over a range of ~ 70mV.

In [103], an auto-referenced power supply noise measurement circuit is reported. The circuit is capable of selectively detecting noises from different bands of frequency spectrum, each due to a different resonance peak in the PDN impedance, thus allowing characterization of noises according to the frequency band. The reference circuit was used to characterize a PCI-Express high speed link on a 0.13  $\mu\text{m}$  CMOS process. The circuit is capable of measuring noise over a range of  $\pm 105$  mV with a resolution of 15 mV. However, due to parasitics, the PDN noise can be characterized only up to 500 MHz.

An on-die droop detector (ODDD) is presented in [82]. The droop detector is capable of analog sensing of high bandwidth power supply noise up to  $\sim 10$ GHz. The detector records different type of fluctuations in real time. It is interfaced through a standard low-speed JTAG port, and is suitable for high volume data collection on a system platform. In the ‘high-resolution’ mode, the ODDD can provide a noise voltage resolution as low as  $\sim 7$ mV.

The previously reported techniques require an on-chip circuitry and references in order to characterize the PDN in several different ways. For our feasibility study and system characterization purposes, building and validation of an on-chip circuitry for monitoring noise is an ‘over-kill’ at this stage of the project. A much simpler and a reliable method of characterizing the PDN noise can be realized by using a setup derived from the one used for measuring the high frequency characteristics of the PDN in the previous chapter. This setup will be described in Section 5.2.4.

### **5.2.3 PDN Noise Modeling**

Random power supply noise can only be characterized reliably by multiple measurements and using empirical techniques to capture the statistical variations. A generic Norton model based on the maximum and minimum voltage variations measured on the PDN noise was reported in [83]. A more sophisticated model for full chip power grid simulation was presented in [83]. The method is composed of RLC elements excited by constant voltage sources and switching capacitors. By integrating,

the on-chip model and package model, a seamless model is obtained and a complete, rapid, and accurate core-switching noise analysis can be performed.

Due to the enormous number of noise sources in a microprocessor, one can conclude that the overall noise will tend to a Gaussian process by the central limit theorem [85][79]. Also, since the majority of switching is periodic with respect to the main clock the noise can be considered to be cyclostationary Gaussian noise. Incidentally, cyclostationary noise models have also been proposed for conventional PLC to characterize synchronous components of the noise in the power line [80].

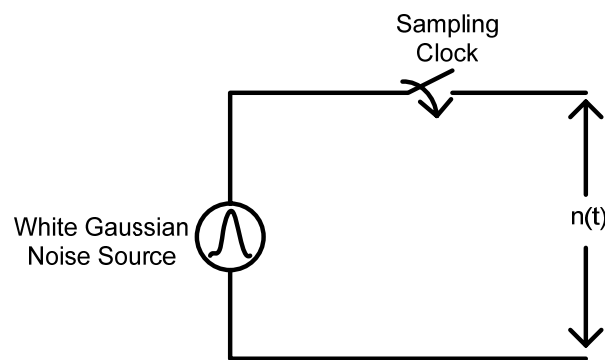


Figure 5.7: Simple cyclostationary noise model

Gaussian cyclostationary noise can be modeled simply as shown in Figure 5.7 by having a white Gaussian noise source model which is sampled periodically [86][87]. Note that the sampling clock need not be the same as the main clock [79]. However, as previously mentioned, analytical models can only serve as approximations and measurements need to be carried out in order to characterize the time domain dynamics of the noise.

White Gaussian noise can be modeled in Matlab and the power level of the noise can be adjusted based on measurements reported previously or by our own measurements on the latest generation of Intel processors. The sampled variations measured on the power supply noise of an Itanium processor was reported in [52]. The average variation is less than  $20\text{mV}_{\text{p-p}}$  (with a core supply voltage of 1.05V) but

sampled noise voltage is observed over a range of  $\sim 70\text{mV}$ . Power Spectral Density (PSD) of power supply noise in a high-speed link transceiver was reported in [79]. In this ASIC, apart from the deterministic components, the power supply noise mostly appears white with a PSD of  $\sim -34\text{ dBV}/(\text{Hz})^{(1/2)}$ . The power spectral density of white Gaussian noise generated in Matlab is shown in Figure 5.8.

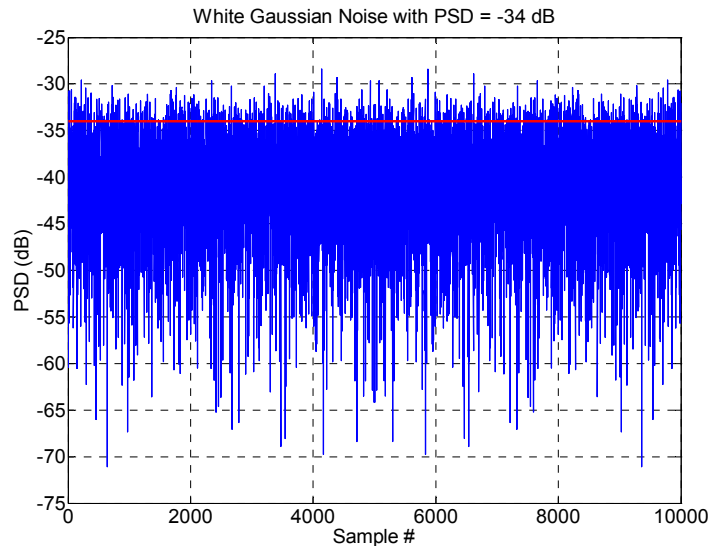


Figure 5.8: PSD of the Gaussian white noise generated in Matlab

#### 5.2.4 Our PDN Noise Measurement Setup

The PDN noise measurement setup for measuring the noise in the PDN is shown in Figure 5.9. The preparation of the part is similar to the part preparation for high frequency characteristics on the PDN. For noise measurement purposes 65 nm Itanium processor and 45 nm Core 2 Duo processor parts were prepared. Using chemical etching and Focused Ion Beam (FIB), a probing hole is made through the back of the die in a flip chip to access a Vcc node on the on-chip PDN. Since the probing hole is made through the back of the die, the first metal layer that is seen is that of M1 metal layer instead of the higher metal layers. This conveniently lets us measure the variation of Vcc voltage exactly at the location of circuitry.

The voltage variations on the PDN were observed on a wide bandwidth (single shot bandwidth = 6 GHz). Again RF picoprobe was used to make contact with the exposed node on the on-chip power grid and a high bandwidth cable was used to connect the probe to the scope. The probe and the high bandwidth cable had bandwidths much beyond 6GHz, therefore the bandwidth of the measurement system was constrained by the scope's bandwidth but based on the results reported in [79] we concluded that 6GHz is quite sufficient for PDN noise measurements.

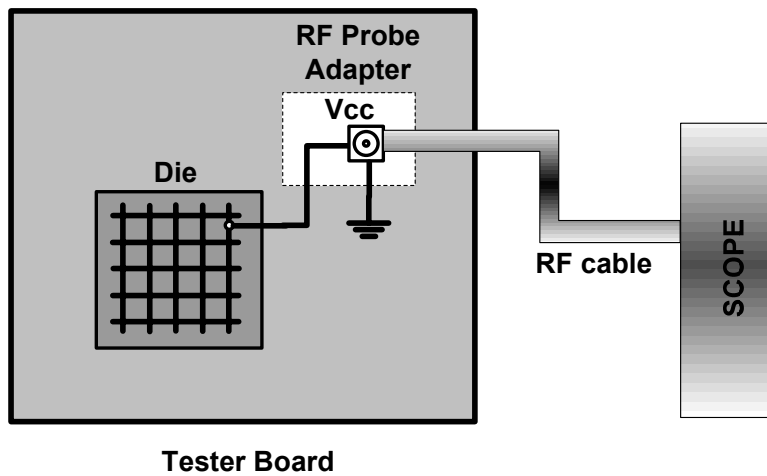


Figure 5.9: PDN noise measurement setup

During full load operation, (operating voltage and application being run on the processor) a 65nm Itanium processor can draw upwards of 100A and a 45 nm Core 2 Duo processor draws more than 50A. The input of the high frequency oscilloscope used for measurements is typically limited to DC current rating of 5A. Therefore, DC blocks are used to limit the input current of the oscilloscopes.

Also in order to be able to probe an active microprocessor, the thermal cooling setup needs to be removed because it limits access to the probing setup used in the noise measurement system. Without the thermal cooling, the processor was run at low supply voltages, smallest operating clock frequency and codes with low activity level

to keep the current levels of the processor pretty low. Typically the supply voltage was limited to the lowest operating level and lowest operating clock frequency. The exact value depends on the sample and is identified by subjecting the part to a functional test at different voltage levels and clock frequencies. For our measurements on the 65 nm Itanium processor and the 45 nm Core 2 Duo processor, the lowest operating clock frequencies were below 1 GHz and the supply voltage was 0.8 V and 0.7 V respectively. At this activity and voltage levels, the drawn current was less than 5 A and the local air cooling was sufficient.

### **5.2.5 PDN Noise Measurements on 65 nm Itanium Processor and 45 nm Core 2 Duo Processor**

Due to the associated thermal and mechanical difficulties with the picoprobe setup, as detailed earlier, the Core 2 Duo part was run at a supply  $V_{cc}$  voltage 0.7V. The 65 nm Itanium part was run at a supply  $V_{cc}$  voltage of 0.8V. The processors were executing a functional test loop, while the measurements were taken. A low frequency component was initially observed on the measured  $V_{cc}$  variations due to the vibrations on the test floor at which measurements were taken. The measured  $V_{cc}$  variations on the 45 nm Core 2 Duo are shown in Figure 5.10 and it can be noticed that the variations are centered on 0.7V. The maximum  $V_{cc}$  variations observed were  $\pm 50$  mV<sub>pp</sub>. The measured  $V_{cc}$  variation is shown in Figure 5.11 and it can be noticed that the variations are centered on 0.8V. The maximum variation was  $\pm 60$  mV<sub>pp</sub> on the 65nm Itanium processor. The worst case variations are used to fix the noise floor in the next section on system level considerations.

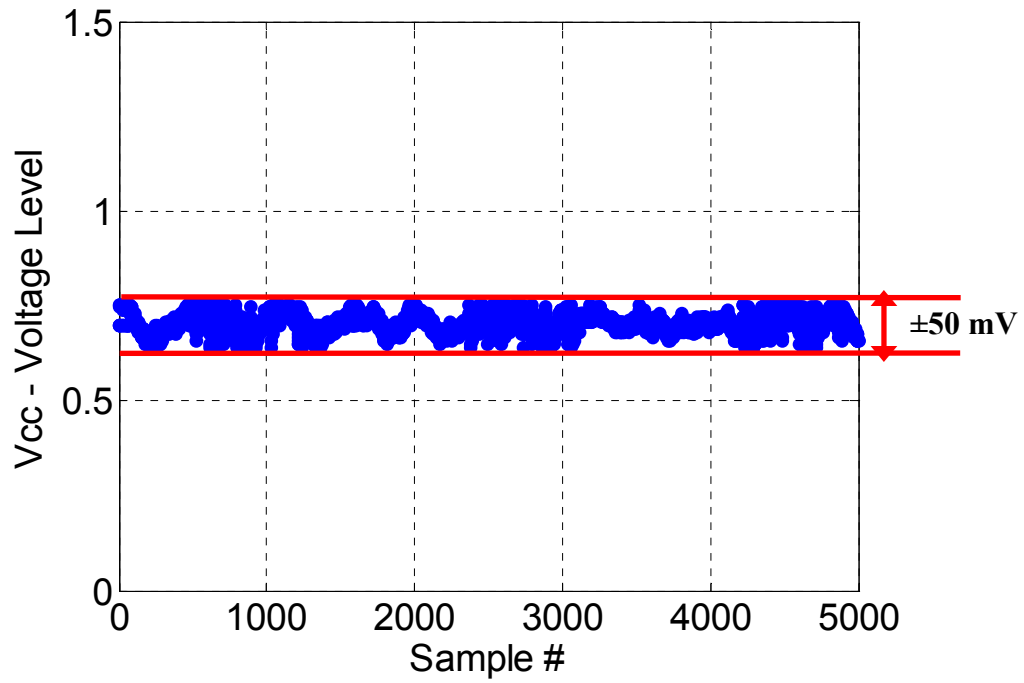


Figure 5.10: Measured PDN noise on 45 nm Core 2 Duo

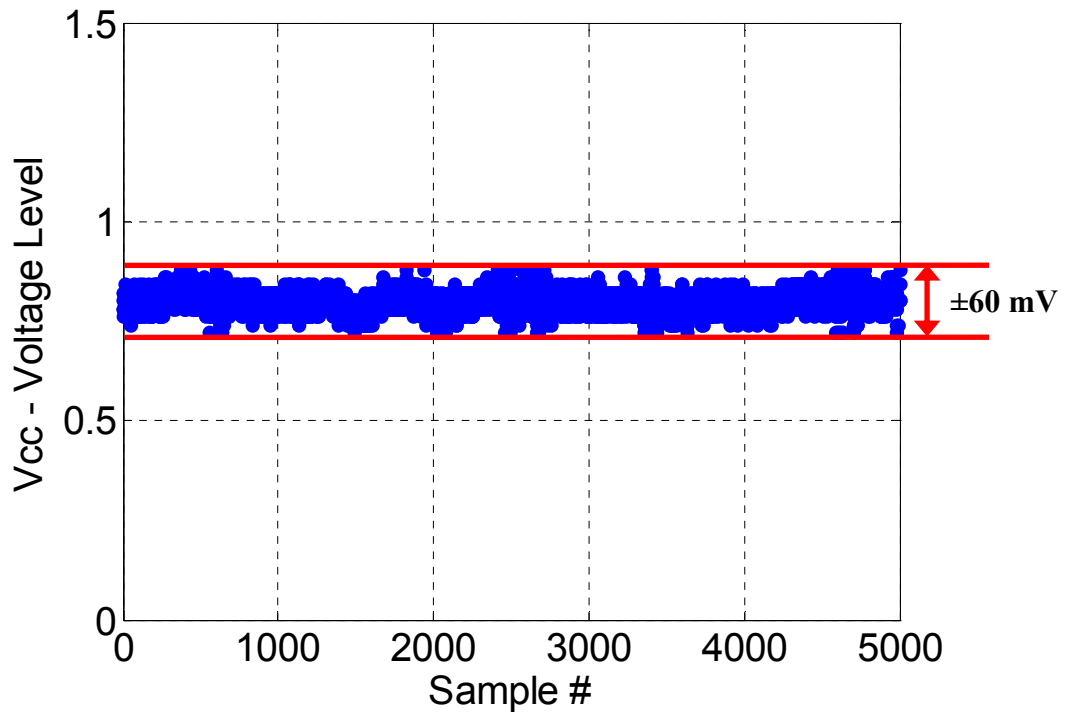


Figure 5.11: Measured PDN noise on 65 nm Itanium processor

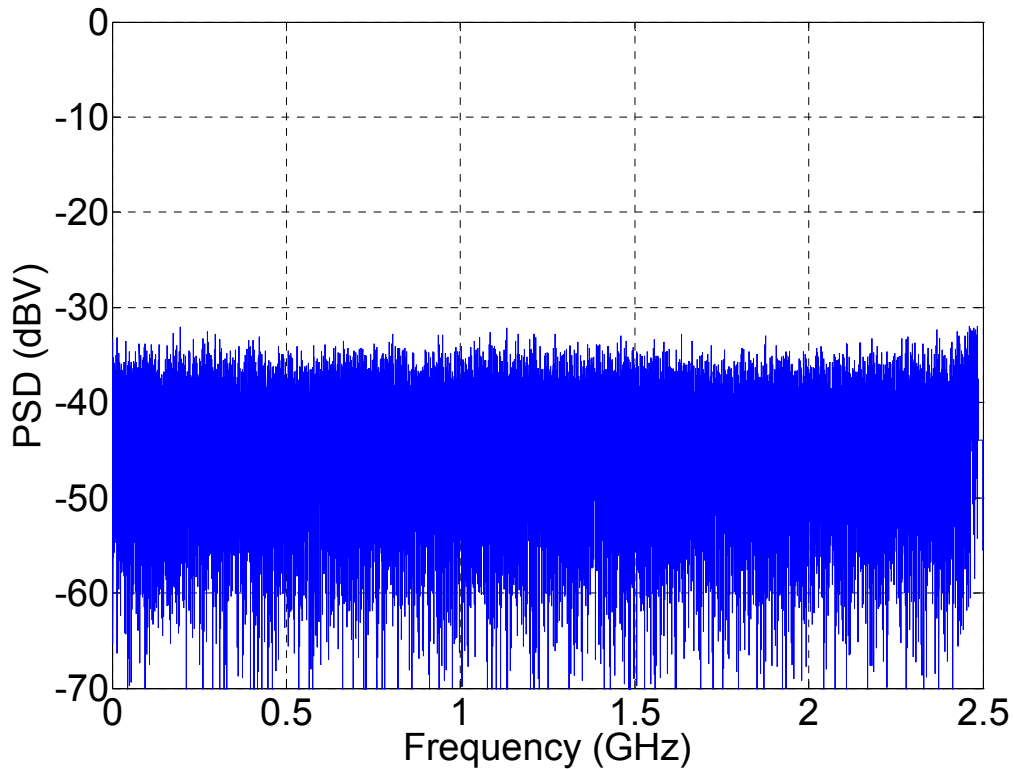


Figure 5.12: PSD of the PDN noise on 45 nm Core 2 Duo

Power spectral density (PSD) of the PDN noise was calculated from the time domain oscilloscope measurements and is shown in Figure 5.12. The oscilloscope was operating at a sampling rate of 5 GSamples/s and therefore the PSD (expressed in dBV) extends to 2.5 GHz. The deterministic components observed at the microprocessor clock frequency were suppressed to separate the switching noise from the deterministic components at microprocessor's internal clocks. From Figure 5.12, one can observe that the PSD of PDN noise is uniform up to 2.5 GHz as expected with a power level of  $\sim -34$  dBV. The power level of PDN noise is utilized for link budget calculations presented in the next section.

### 5.3 System Design Considerations

This section presents the link budget calculations, appropriate modulation schemes, impact of pulse shapes on interference and considerations for interference mitigation and co-existence.

#### 5.3.1 Link Budget Calculations

The signal to noise ratio (SNR) at the receiver block can be expressed as in

$$SNR_{DR} = SIG_{IN} - PL_{dB} - NF \quad (5.1)$$

where  $Sig_{IN}$  is the signal power at the input,  $PL_{dB}$  is the path loss through the PDN channel and  $N_{floor}$  is the power supply noise floor (all quantities expressed in decibels). For a more detailed analysis of the link budget of a UWB system one can refer to [88].  $PL_{dB}$  is estimated by Referring to the path loss variation with frequency of the PDN channel in the processor under consideration. Noise Floor is based on the measurements presented in the section 5.3. A sample link budget calculation for communication over the Core 2 Duo PDN is shown in Table 5.1.

Table 5.1: Sample link budget for communications on Core 2 Duo PDN

<b>Sig<sub>IN</sub></b>		<b>N<sub>Floor</sub></b>		<b>Sig<sub>DR</sub></b>		<b>SNR<sub>DR</sub> (dB)</b>
<b>mV</b>	<b>dBm</b>	<b>mV</b>	<b>dBm</b>	<b>mV</b>	<b>dBm</b>	
100	40.0	50	33.98	8.91	19.00	-14.98
200	46.02	50	33.98	17.82	25.02	-8.96
400	52.04	50	33.98	35.64	31.04	-2.98
600	55.56	50	33.98	53.45	34.56	0.58

For the Core 2 Duo PDN, the path loss was fixed at 21 dB and the noise floor at the 50mV based on the measurements. From Table 5.1, it can be noted that the amplitude of the pulse at the input needs to be as high as 600mV to get a positive SNR at the output. Although, communication is still possible even if the SNR is negative but

that will require a strong coding scheme in the transmitter and a corresponding increase in the hardware complexity of the DR block, but the increase in complexity will be mostly in the digital circuitry of the receiver block.

### 5.3.2 Modulation Techniques for PDN communications

Two different modulation schemes were considered for communication over the PDN channel; Binary Phase Shift Keying (BPSK) and the Phase Shift Modulation (PSM). In this section, the two modulation schemes are revisited and the pros and cons are discussed with respect to communication over PDN.

#### 5.3.2.1 Binary Phase Shift Keying (BPSK)

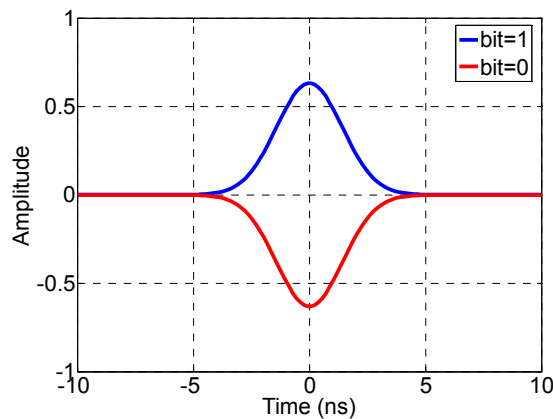


Figure 5.13: Binary Phase Shift Keying

BPSK modulation scheme is illustrated in Figure 5.13. In this modulation, positive and negative pulses (usually Gaussian, raised cosine or their derivatives) represent the two possible bit values [5]. Gaussian or their higher order derivatives can be easily generated using digital schemes and tunable delay elements [89]. Binary phase shift keying is simple and energy efficient. Since reliable communication is

possible with simple transmitter and receivers, this modulation scheme is a good choice for communication over the PDN.

### 5.3.2.2 Pulse Shape Modulation (PSM)

One of the main drawbacks of BPSK is not very robust in the presence of clock jitter i.e. the Bit Error Rates (BER) increases dramatically especially if peak detection based receivers are used. The transmitters and receivers for the proposed system would be located at widely varying locations on the die and hence the clock skew and jitter is a cause for major concern. Therefore we consider another modulation scheme viz. Pulse Shape Modulation (PSM) which is highly robust in the presence of clock jitter. PSM scheme is show in Figure 5.14. In this modulation, different orthogonal pulse shapes are used for sending different bit values. The modified Hermite Polynomial (MHP) shaped pulse and its higher order derivatives are preferred due to their ease of generation apart from their orthogonal properties [15]. The MHP pulses of different order can be expressed as in (5.2)

$$h_n(t) = (-1)^n e^{-\frac{t^2}{4}} \frac{d^n}{dt^n} \left( e^{-\frac{t^2}{2}} \right) \quad (5.2)$$

Where  $n = 0, 1, 2, \dots$  and  $-\infty < t < \infty$ . In Figure 5.14, second and third order MHP pulses are shown (the number of zero crossings determine the order of MHP pulse).

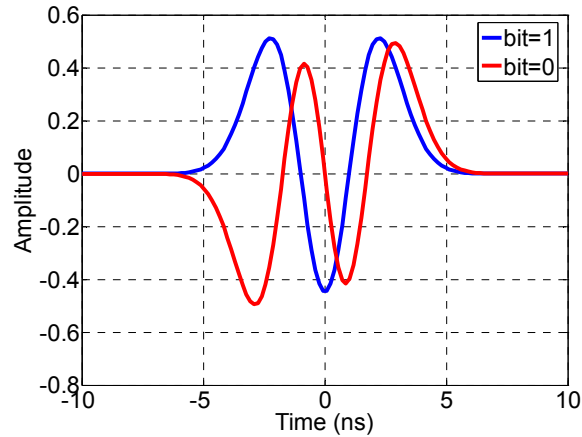


Figure 5.14: Pulse Shape Modulation

### 5.3.2.3 Pulse Position Modulation (PPM)

Apart from these two modulation schemes the Pulse Position Modulation (PPM) was also considered. The main advantage of pulse position modulation is that it requires only uni-polar pulses. In PPM narrow negative going impulses on the PDN can be used for signaling which simplifies pulse generation without the need for overdriving the PDN however, for internal transmission and reception it would require very precise control of the position (timing) of the pulses. Precise timing control would increase the complexity of the internal transmitters/receivers and hence PPM was overlooked.

### 5.3.3 Impact of Pulse Shapes on Interference

Apart from the modulation schemes and link budget the extra ‘noise’ added by the proposed communication method should be below the typical noise floor fixed by the signal integrity concerns, so the communication method does not interfere with the normal operation of the microprocessor (i.e. cause any signal integrity issues due to supply voltage variations).

Simulations were carried out in Matlab to compare the root mean square (RMS) voltage levels of the different pulse shapes in consideration for communication over the PDN. The basic premise is if the RMS voltage levels of the pulses are below the worst case variations, the proposed communication method over the PDN would cause no interference to normal operation of the microprocessor. For pulse based ultra-wideband (UWB) communications over the PDN, currently two modulation schemes are being studied. To achieve high energy efficiency Binary Pulse Shift Keying (BPSK) is being considered and the Pulse Shape Modulation (PSM) technique because of its robustness to clock-jitter. The different pulse shapes appropriate for BPSK are the Gaussian pulses and their derivatives due to their ease of generation and reception. These pulse shapes are shown in Figure 5.15. In PSM, the different pulse shapes considered are the Modified Hermite Polynomials (MHP) mainly for their orthogonal properties. The different MHP pulses from 0<sup>th</sup> order to 3<sup>rd</sup> order are shown in Figure 5.16.

Peak amplitudes of the pulses were restricted to be less than 5% (~50 mV for a nominal Vcc of 1 V) of the core Vcc voltage. The duration of the pulses has to be as small as possible to make them resemble glitches in the core Vcc level that occur normally during switching activities. Pulse duration was fixed at 100ps to ease the circuit design of internal transmitter and receivers in deep submicron technologies. Simulations results of the RMS values for the different pulse shapes are shown in Table 5.2. Results indicate that the RMS values of the different pulse shapes vary over a fairly small range from 17 mV to 23 mV.

Recall that noise levels measured on Intel's 45 nm Core2Duo processor and the 65 nm Itanium processor were presented in Section 5.2. The worst case variation was ~ ±50 mV on the 45 nm Core 2 Duo processor and ±60 mV on the 65nm Itanium processor. The calculated RMS values remain well below the typically observed variations on the core Vcc voltage levels in microprocessors during normal operation. One can conclude that by using pulses with peak amplitude < 5% of nominal Vcc voltage level and as short a duration as possible, interference to normal operation due to pulse based communication method over the PDN can be made non-existent. RMS

voltage level of the pulses remain well below ( $< 25\text{mV}$ ) typical noise levels observed in the microprocessor PDN thereby causing no interference to normal operation.

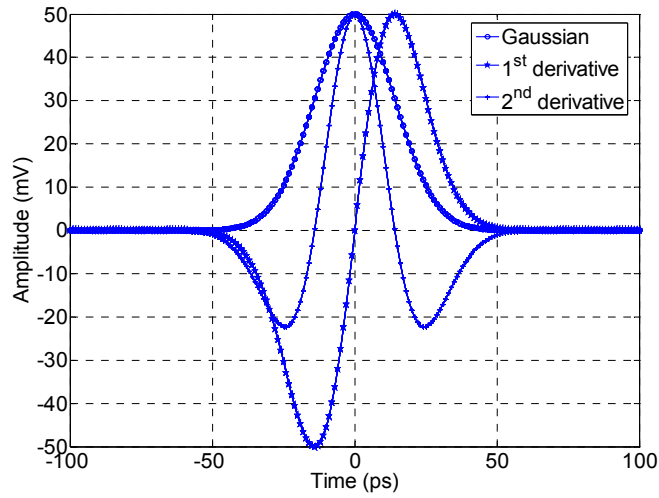


Figure 5.15: Pulse shapes for BPSK

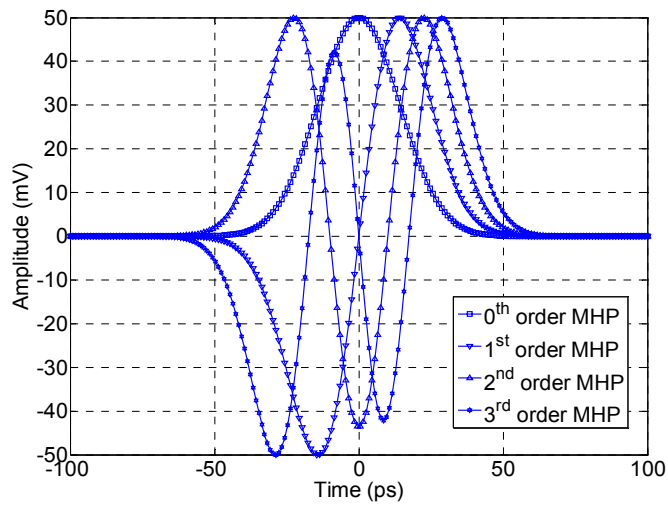


Figure 5.16: Pulse shapes for PSM

Table 5.2: RMS voltage levels of different pulse shapes

<b>Pulse Peak Amplitude = 50 mV</b>	
<b>Pulse Duration = 100 ps</b>	
<b>Pulse Shape</b>	<b>V<sub>RMS</sub> (mV)</b>
Gaussian	40.0
Gaussian (1 <sup>st</sup> derivative)	46.02
Gaussian (2 <sup>nd</sup> derivative)	52.04
1 <sup>st</sup> order MHP	55.56
2 <sup>rd</sup> order MHP	20.60
3 <sup>rd</sup> order MHP	21.79
4 <sup>th</sup> order MHP	22.56

### 5.3.4 Narrow Band Interference Mitigation and Co-existence

Narrow band interference for the proposed communication approach over a PDN arises from deterministic components located at the main clock and at the PLL reference clock frequencies. The interference to the PDN communication can be mitigated by using spreading. Note that the associated increase in bandwidth is not a major concern in our approach [90]. Spreading also helps to reduce the power spectral density over the information bandwidth and reduces the interference to normal operation of the microprocessor. The study of spreading techniques and possible codes will be a part of the future work on this research.

## 5.4 Chapter Summary

In section 5.1, a channel model is developed based on the S-parameter measurements taken for feasibility study. By using the path loss and phase response of the PDN channel, the impulse response can be derived. Using the impulse response, the channel response for any input pulse can be calculated.

In section 5.2, noise characteristics usually observed on the microprocessor PDN is described. Several previously noise measurement techniques reported in literature is

presented. Modeling of PDN noise based on noise measurements is discussed. Our measurement setup for measuring noise in the PDN is described. Finally, results of the noise measurements carried out on the 65 nm Itanium processor and the 45 nm Core 2 Duo processor is presented.

The different system level issues are studied in section 5.3. A link budget was developed based on the path loss measurements, as well as the noise levels observed on the PDN. The different modulation schemes and the trade-offs are studied with respect to the PDN communications. Also, the impact of interference caused by proposed communication method as a function of different pulse shapes was studied using Matlab simulations. Finally, methods for mitigating strong narrowband interference are discussed.

## **Chapter 6: Receiver and Transmitter Design**

In this chapter, a circuit design approach for sending and receiving impulse modulated data from power lines is described. A receiver design is proposed and its circuit level details are described. The performance of the receiver is evaluated through simulations in TSMC 0.18 $\mu$ m CMOS process. A transmitter design is proposed and its circuit level details are described. The performance of the transmitter is evaluated through simulations in TSMC 0.18 $\mu$ m CMOS process.

### **6.1 Receiver Design**

#### **6.1.1 Challenges in Receiver Design**

There are several challenges in the design of a data recovery block for communication over a microprocessor's PDN. Firstly, a data recovery block should be able to recover data from input signals whose voltage level exceeds its supply voltage (VDD). This is because the voltage level of a positive pulse imposed on the VDD is greater than the supply voltage of the data recovery block (which is also VDD). This situation is seldom encountered in circuit design. Secondly, the data recovery block should have high sensitivity with low offset, as the amplitude of pulses is small relative to the VDD level. Further, a microprocessor PDN is extremely noisy due to the enormous switching activity taking place in the die. Therefore the design should have high noise immunity. Finally, for the application envisioned to be feasible, the design should be digital-process friendly with minimal area and power overhead.

#### **6.1.2 Proposed Receiver/Data Recovery Block**

This section describes the general approach for receiver design and the circuit level implementation of the different blocks in the receiver.

### 6.1.2.1 Our Approach

From the perspective of a sensing circuit, narrow pulses superimposed on the supply voltage are high speed variations on the supply voltage level. Therefore, a sensing circuit has to translate the power supply voltage variation to a voltage variation offset by the output DC level of the sensing circuit. In fact, it is a common design practice to isolate the circuit output from power supply variations. Power Supply Rejection Ratio (PSRR) indicates the level of isolation of a circuit output from the power supply variations, and a larger PSRR is typically desired.

Our approach is to deliberately degrade the PSRR of a sensing circuit, so that the variations on the supply voltage level would appear at the sensing circuit output. We set the DC output voltage level of the sensing circuit at  $0.5V_{DD}$ , and a positive (negative) pulse on  $V_{DD}$  will increase (decrease) the output voltage of the sensing circuit. The variation can then be amplified and regenerated to digital levels by a positive feedback latch similar to the technique used in DRAM cells [110][111]. On the downside, degrading the PSRR would mean that accompanying power supply variations would also be transferred to the output of the sensing circuit. However, as long as the high speed variations offset by  $V_{DD}$  are transferred to the circuit's output and the offset level is lowered the sensing scheme would suffice. Noise immunity can be improved by using strong coding (decoding) techniques in the back end or by using a differential signal path in the receiver.

#### 6.1.2.1.1 Sensing Circuit

The sensing scheme used for the proposed data recovery block is shown in Figure 6.1. It is a conventional common source amplifier with a diode-connected load. The input to the circuit is held at a constant voltage  $V_{bias}$ . A systematic sizing procedure for degrading the PSRR of the sensing circuit is described below.

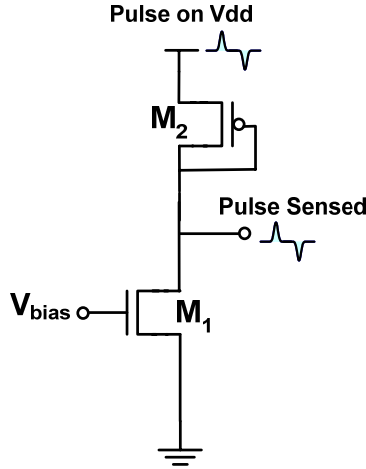


Figure 6.1: Sensing scheme in the receiver

The PSRR of a common source amplifier shown in Figure 6.1 can be expressed as in (6.1).

$$PSRR = \frac{V_o}{V_{dd}} \approx \frac{1}{2 \cdot g_{m(M_2)} \cdot r_{o(M_1)}} \quad (6.1)$$

In-order to degrade the PSRR to its absolute worst, one has to maximize the product of  $g_{m(M_2)}$  and  $r_{o(M_1)}$ . The transconductance of  $M_2$ ,  $g_{m(M_2)}$  is expressed as shown in (6.2).

$$g_{m(M_2)} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (6.2)$$

The output resistance  $r_{o(M_1)}$  is expressed as in (6.3),

$$r_{o(M_1)} = \frac{1}{\lambda I_D} \quad (6.3)$$

From (6.2) and (6.3) we observe that the product  $g_{m(M_2)} \cdot r_{o(M_1)}$  is inversely proportional to  $\sqrt{I_D}$ . Therefore, PSRR of the sensing circuit is degraded by reducing the current  $I_D$  through the sensing circuit.

However, the DC output voltage level of the sensing circuit is fixed at  $0.5V_{DD}$  for regenerating the sensed pulse to digital levels. This, in turn, fixes the overdrive voltage of  $M_2$ . Therefore, the minimum current  $I_D$  is obtained by using minimum W/L ratio for  $M_2$ . The bias voltage  $V_{bias}$  and the W/L ratio of the  $M_1$  are calculated to make sure that the transistor  $M_1$  remains in saturation.

#### 6.1.2.1.2 Buffer Amplifier with Offset Cancellation

The sensing circuit is single-ended and buffer amplifier is used to increase the sensitivity as well as to convert the single ended path to differential to improve the noise immunity of the data recovery block. The buffer amplifier is shown in Figure 6.2. The buffer amplifier also includes an offset cancellation mechanism by including transistors  $M_1$  and  $M_2$ . During the low phase of the clock, when  $M_2$  is off and  $M_1$  is on, the output voltage of the buffer amplifier can be expressed as in (6.4)

$$V_{out+} - V_{out-} = K(V_{sco} - V_{bias} - V_{offset}) \quad (6.4)$$

where  $V_{out+}$  and  $V_{out-}$  are the outputs of the buffer amplifier,  $V_{sco}$  is the output of the sensing circuit,  $V_{bias}$  is the reference voltage of the buffer amplifier,  $V_{offset}$  is the input-referred offset voltage of the buffer amplifier and  $K$  is the gain of the buffer amplifier. During the low phase of the clock, when  $M_1$  is off and  $M_2$  is on, the input and negative output of the buffer amplifier are shorted together. Therefore,

$$V_{out-} = V_{sco} \quad (6.5)$$

Note that during this phase, the sensing circuit is disconnected from the input of the buffer amplifier and  $V_{sco}$  is the voltage to which the input node of the buffer amplifier was charged at the end of the previous clock phase. Using (6.5) in (6.4), and solving for the voltage at the input node of the buffer amplifier i.e.  $V_{sco}$  in this case, we get

$$V_{sco} = \left( \frac{V_{out+}/K + V_{bias} + V_{offset}}{1 + 1/K} \right) \quad (6.6)$$

For large values of  $K$ , we have

$$V_{sco} \approx V_{bias} + V_{offset} \quad (6.7)$$

From (6.7), one can infer that the input node of the buffer amplifier which is connected to the output of the sensing circuit is charged to the reference voltage of the buffer  $V_{bias}$  and the input referred offset voltage of the buffer  $V_{offset}$ . Therefore, irrespective of the offset voltage and sufficiently large values of gain  $K$ , the offset voltage is stored at the input node of the buffer amplifier. During the following low phase of the clock, the output voltage is as expressed in (6.4) and the stored offset voltage is eliminated.

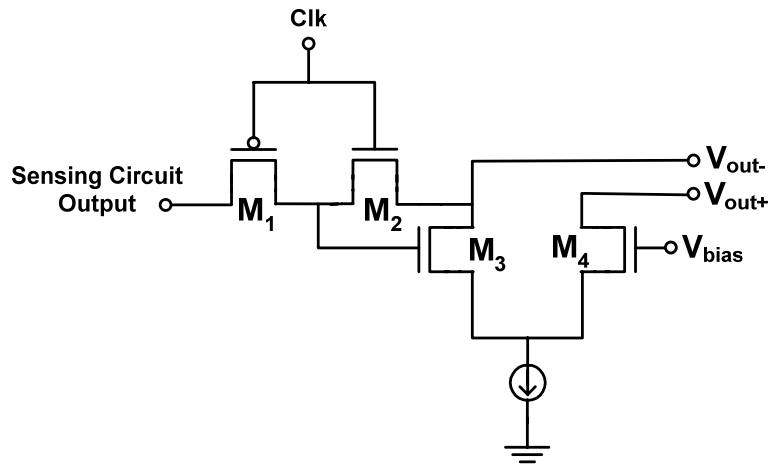


Figure 6.2: Buffer amplifier in the receiver

### 6.1.2.1.3 Latch

In order to regenerate the sensed pulses to digital levels, the buffer amplifier is followed by a differential latch shown in Figure 6.3 [91]. The latch is basically two inverters formed respectively by  $M_1, M_3$  and  $M_2, M_4$  connected back-to-back in a positive feedback latch. Device  $M_5$  connected between the inputs of the inverters and controlled by the Clock is used to switch the latch between the reset and the latching

(regeneration) phase. Based on the whether input  $V_{in+}$  is greater than  $V_{in-}$  or vice versa, the output  $V_{out+}$  is regenerated to digital ‘1’ and output  $V_{out-}$  is regenerated to a digital ‘0’ or vice versa. The regeneration time is extremely low and of the order of a few ‘time-constant’s due to positive feedback mechanism in the latch.

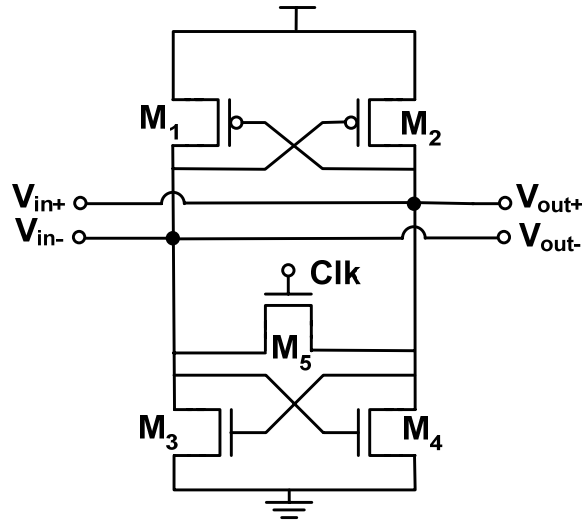


Figure 6.3: Latch in the receiver

### 6.1.2.2 Overall Architecture

The entire data recovery block is shown in Figure 6.4 [92]. The sensing circuit is followed by a differential amplifier to amplify the sensed variations appearing at the sensing circuit output. The differential amplifier compares the sensed variation with a constant reference voltage  $V_{bias}$  and converts the single ended signal path to differential. By proper sizing of  $M_5$  and  $M_6$ , the same voltage  $V_{bias}$  can be used as a reference voltage for the differential amplifier as well.

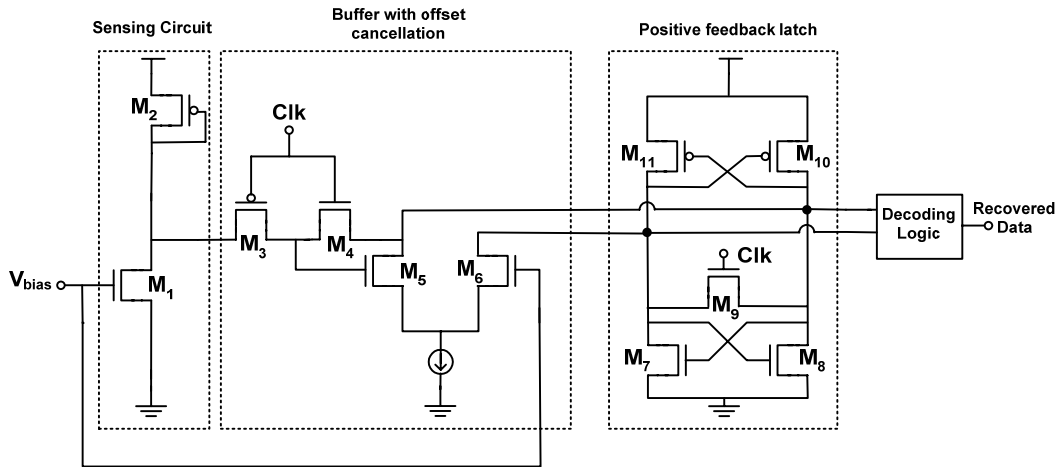


Figure 6.4: PDN communication receiver

Differential input to the latch helps to improve noise immunity as well as reduce the effect of offset variations. To reduce the effect of offset at the input of the latch, a conventional offset cancellation scheme is implemented using transistors  $M_3$  and  $M_4$ . During the offset cancellation phase, with the clock high,  $M_4$  is turned on, and the drain of  $M_5$  is connected to its gate. Simultaneously,  $M_3$  is turned off, and the gate of  $M_5$  is isolated from the output of the sensing circuit. In this configuration, the input offset of the differential amplifier is stored in the parasitic gate-source capacitance of  $M_5$  [10]. During the low-phase of the clock, the stored input offset is subtracted from the differential input and amplified as explained in section 6.1.2.1.2. Finally, a positive feedback latch rapidly regenerates the differential amplifier outputs to digital levels. The built-in sampling switch  $M_9$  in the latch samples the amplifier outputs at the falling edge of the clock. Inverter-based buffers are placed at the output of the data recovery block in-order to pull the output of the latch to the supply rails.

The clock for the data recovery block can be derived from the main microprocessor clock. A stable band-gap reference would be required to generate  $V_{\text{bias}}$  internally, and several data recovery blocks could share a single reference.

### 6.1.2.3 Performance Evaluation

The proposed data recovery block was simulated with the target technology of TSMC 0.18  $\mu\text{m}$  CMOS process under the supply voltage of 1.8 V. The variation in the power supply voltages were modeled using a piece-wise linear (PWL) source. In the definition of the PWL source, positive and negative going 90 mV pulses with duration of 300 ps were superimposed on the 1.8V level. Results of transient simulation are shown in Figure 6.5.

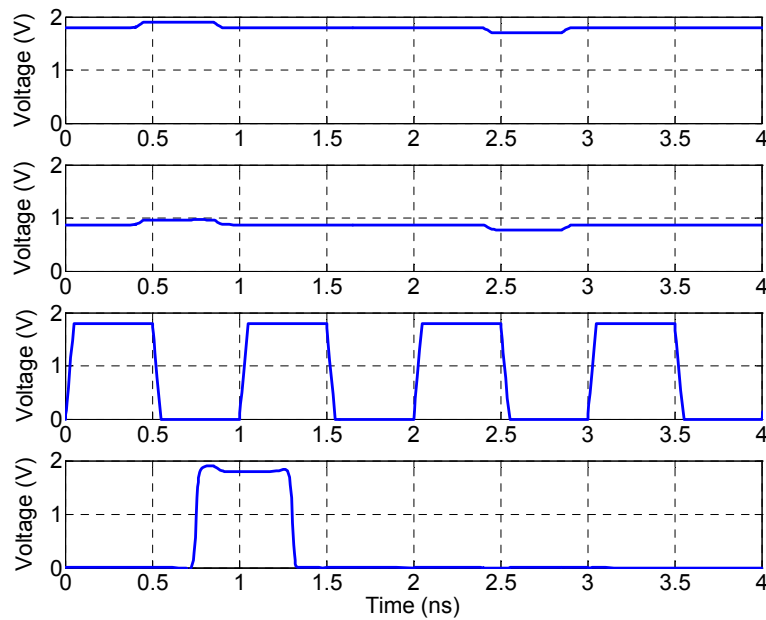


Figure 6.5: Operation of the receiver

The first waveform shows the PWL source on the global VDD, and the second waveform shows the sampling clock operating at 1 GHz. The third waveform shows the voltage at the output of the sensing circuit. It can be seen that the variations on the supply voltage are translated into the output signal variations. Also note that the DC voltage level of the sensing circuit output is set at 0.9 V. The last one shows the overall

output of data recovery block. Note that positive pulses on the supply voltage are regenerated to logic ‘1’s and negative pulses are regenerated to logic ‘0’s.

The offset cancellation scheme implemented on the differential amplifier was evaluated using Monte Carlo analysis as well as mismatch and process variation models in the TSMC 0.18  $\mu\text{m}$  process library [97]. With the process variations set at  $3\sigma$ , the worst case offset observed at the input of the latch was less than 20 mV. The performance of the data recovery block is summarized in Table II.

Table 6.1: Performance summary of receiver

Pulse Amplitude	90 mV
Pulse Duration	300 ps
Clock Rate	1 GHz
Input Offset Variation	< 20 mV
Power consumption	2.8 mW

## 6.2 Transmitter Design

This section describes the approach and circuit level implementation of the proposed internal transmitter.

### 6.2.1 Challenges in Transmitter Design

The main challenge in the pulse generator design is to use digital process friendly circuits to generate positive and negative impulses required in BPSK and PSM schemes without the use of inductors and transformers. On the output stage, the main challenge is to be able overdrive the PDN in a power efficient manner.

## 6.2.2 Our Approach

The overall block diagram of the internal transmitter is shown in Figure 6.6. The transmitter consists of an internal pulse generator and an output stage for superimposing the pulse (i.e. overdriving) on the PDN. The sub-circuits of the transmitter are explained in more detail in the subsequent sections.

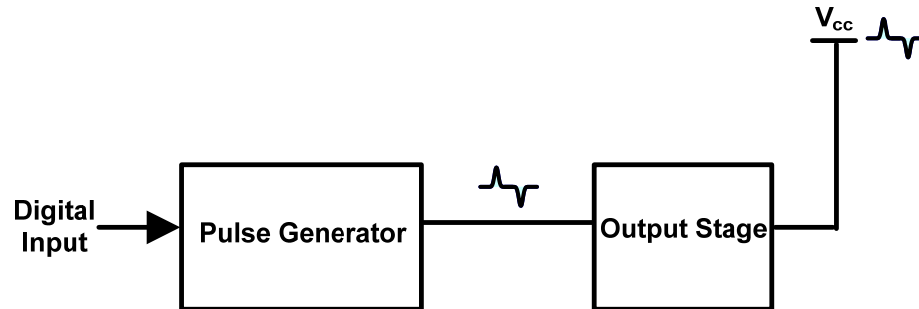


Figure 6.6: Block diagram of the transmitter

### 6.2.2.1.1 Pulse Generation Principle

All the previously reported UWB transmitters for BPSK modulation use inductors or transforms to generate small duration pulses with both negative and positive excursions [93]-[95]. In our transmitter, we avoided the use of inductors by using a charging/discharging method to produce positive and negative excursions on the output node. The pulse generation principle is illustrated in Figure 6.7. The pulse generator shown in Figure 6.7 has three charge/discharge stages. The charging (discharging) occurs when either PMOS (NMOS) transistor is turned on. The delay between the stages is used to control the time between the charging and discharging phases. The shape of the pulses can be tuned intricately by controlling the delays as well as drive strength of the charging (discharging) stages.

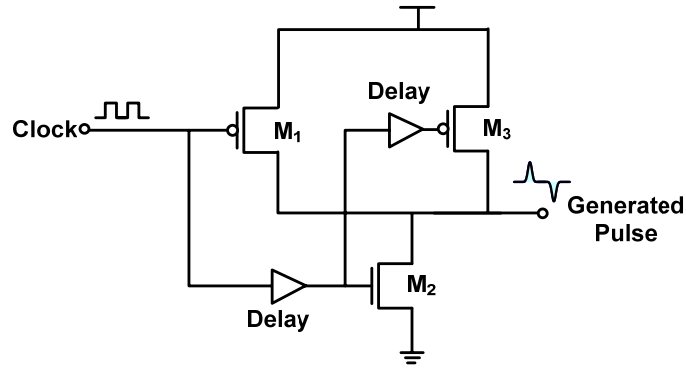


Figure 6.7: Pulse generation principle

Recall from section 5.3.2, pulse shapes considered for PDN communication are Gaussian pulses, their derivatives and the modified Hermite polynomials. The pulses differ by varying number of positive and negative excursions depending on the order of derivative. The delays between the positive and negative excursions and their slope determine the pulse shape. Therefore, the pulse generation principle illustrated in Figure 6.7 is adequate to generate Gaussian pulses, modified Hermite polynomials and their derivatives.

### 6.2.2.1.2 Output Driver

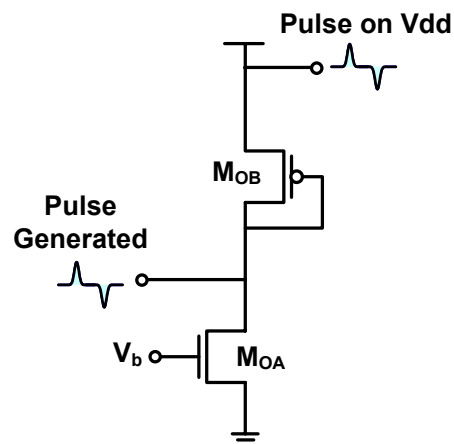


Figure 6.8: Output driver of the transmitter

The output driver of the transmitter is shown in Figure 6.8. The problem of over-driving the PDN can be solved by an approach which works in reverse of sensing scheme of the receiver shown in section 6.1.2.1.1, i.e. the input and output of the sensing circuits are reversed. The generate pulse is applied to the drain of  $M_{OA}$  and the isolation between the drain of  $M_{OA}$  and the  $V_{dd}$  (PSRR) is degraded by the sizing of transistor  $M_{OB}$  and the current in the over-driving stage as in the case of receiver's sensing circuit design. The output driver is much bigger in terms of area and power in order to supply (or sink) a large current to overdrive the PDN. Since the power distribution network is a low impedance network, a large amount of current needs to be driven into the network to generate even small voltage variations.

### 6.2.2.1.3 Overall Architecture of the BPSK transmitter

The complete BPSK transmitter is shown in Figure 6.9. The BPSK transmitter's pulse generator is based on pulse generation principle illustrated in Figure 6.7 and requires only one stage of charging (discharging) assuming a Gaussian monopulse is the pulse shape utilized. Depending on the digital input data, transistor  $M_2$  ( $M_1$ ) sources (sinks) current to (from) the load in order to generate positive (negative) going pulses required for BPSK modulation. The pulse shape can be better controlled by sizing of  $M_1$  ( $M_2$ ).

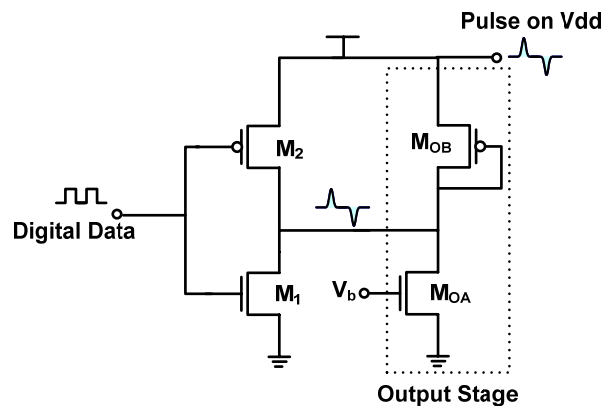


Figure 6.9: BPSK transmitter

#### 6.2.2.1.4 Overall Architecture of the PSM transmitter

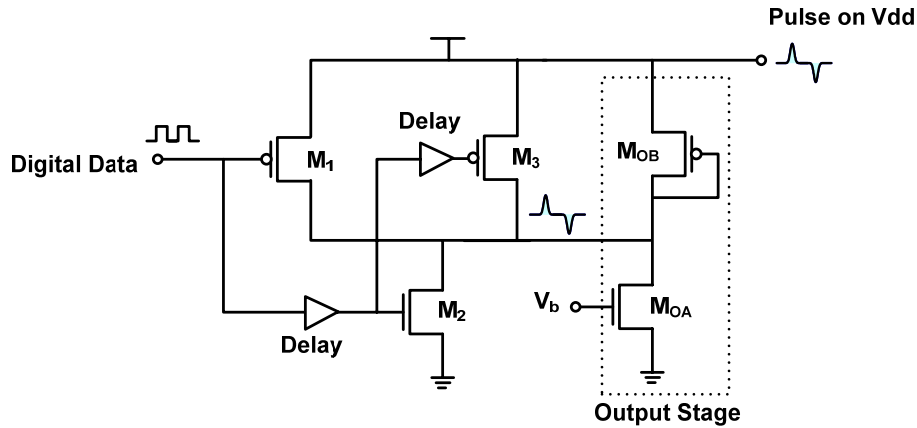


Figure 6.10: PSM transmitter

The circuit level implementation of the PSM pulse generator is shown in Figure 6.10. In this case also, the same pulse generation principle illustrated in Figure 6.7 is utilized. Delayed versions of the digital pulse is generated and they are used to consecutively source (sink) to (from) the load depending on the excursions on the pulse shape modulation. The circuit shown in Figure 6.10 generates a second order PSM pulses because the pulse generated has two zero crossings. Higher order and lower order PSM pulses can be generated by increasing or decreasing the number of charging/discharging stages and delay elements.

Note that, unlike the BPSK transmitter, which can generate the two different pulse shapes required for BPSK with a single circuit, the PSM transmitter requires two different circuit implementations for generating Hermite polynomials of different order. As mentioned earlier, the circuit shown in Figure 6.10, generates a second order modified Hermite polynomial. To generate a third order modified Hermite polynomial, an additional charge (discharge) stage would be required. The two pulse generators can be alternately activated depending on the digital data to be transmitted.

### 6.2.3 Performance Evaluation

The PSM transmitter shown in Figure 6.10 was implemented in TSMC 0.18  $\mu\text{m}$  CMOS process and simulated with Cadence design tools. For the PDN, in the interest of reducing the simulation time, a simple lumped PDN model was used [22]. The simulation results are shown in Figure 6.11. For each bit of data, a digital pulse is generated. The digital pulse and its delayed versions are shown in the first waveform. The second waveform shows the output of the pulse generator. The inductance in the PDN model produces additional ringing effects seen in the pulses. Note that the pulses are centered on 0.82V and the amplitude is  $\sim 70\text{ mV}_{\text{pp}}$ . The last waveform shows the pulses superimposed on the supply voltage level and is centered on  $\sim 1.8\text{V}$ . Again, the output pulse voltage level is  $\sim 70\text{mV}_{\text{p-p}}$ .

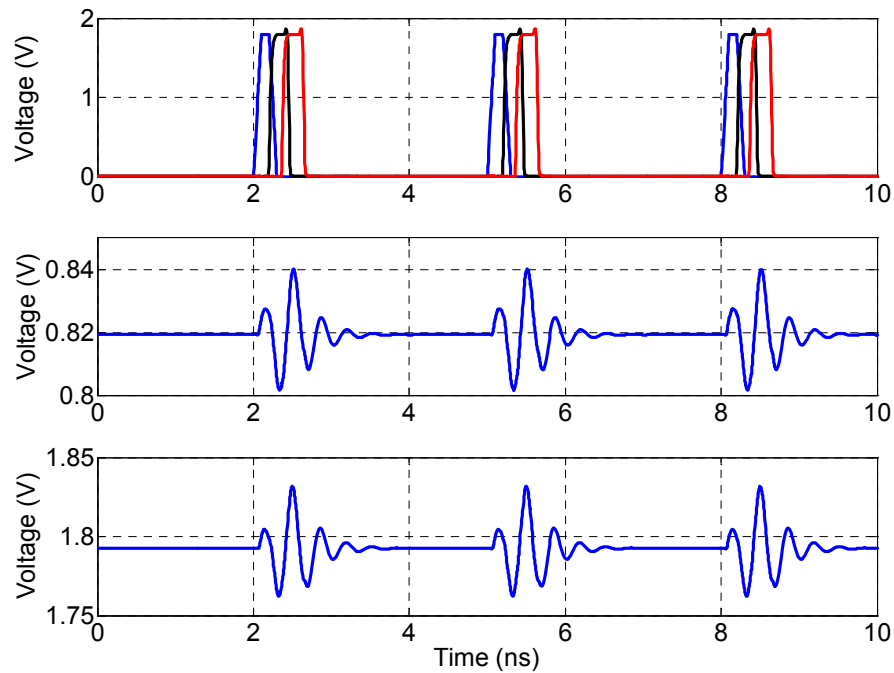


Figure 6.11: Operation of the transmitter (2<sup>nd</sup> order PSM pulse generator)

Table 6.2: Performance summary of transmitter

Pulse Amplitude	70 mV <sub>p-p</sub>
Pulse Duration	300 ps
Power consumption (BPSK)	4 mW
Power consumption (PSM 2 <sup>nd</sup> order)	7 mW
Power consumption (PSM 3 <sup>rd</sup> order)	8 mW

Performance of the internal transmitter for the different pulse shapes and for modulation schemes is summarized in Table 6.2. Comparing with Table 6.1, one can notice that the transmitter is considerably more power-hungry than the receiver. Also, the BPSK transmitter consumes about one half of the PSM transmitter. A single BPSK transmitter can generate both pulses required for modulation, but a PSM transmitter would require a 2nd order and a 3rd order pulse generator. However, PSM modulation increases the reliability of communication over the PDN and hence the trade-off.

### **6.3 Chapter Summary**

In section 6.1, challenges in receiver design are discussed. An approach for recovering data sent over power lines is described and the different circuit blocks in the receiver are discussed in detail. Performance of the receiver is evaluated by simulations in TSMC 0.18  $\mu\text{m}$  CMOS process.

In section 6.2, challenges in transmitter design are discussed. An approach for efficiently driving the power lines in a microprocessor is discussed. The various circuit blocks in the transmitter are discussed in detail. Performance of the transmitter is evaluated through simulations in TSMC 0.18  $\mu\text{m}$  CMOS process.

## **Chapter 7: Summary & Future Work**

A novel communication method over the power distribution network had been proposed previously at VTVT and in this work, the feasibility of the proposed method through modeling and measurements. Further, Channel modeling studies were conducted and conclusions were derived on the modulation techniques, pulse shapes and also interference caused by the proposed method. Finally, a circuit design approach for communication over the power distribution network was proposed. A receiver design for recovering the data modulated with narrow impulses from the power lines was proposed and evaluated through simulations in TSMC 0.18 $\mu$ m CMOS process. A novel transmitter design for driving the low impedance PDN in a power efficient manner was proposed and evaluated through simulations in TSMC 0.18 $\mu$ m CMOS process.

### **7.1 Summary**

Chapter 1 provides the motivation behind the proposal to communicate over the power lines of microprocessor's power distribution network. As the complexity of the microprocessors is increasing at a rapid rate, the accessibility to core logic is going down at a remarkable rate. The accessibility is almost non-existent on an operating processor because the self test elements are mostly removed. Using the power lines as data paths provide ubiquitous accessibility to core logic with remarkably little area and design overhead.

Chapter 2 discusses the relevant background information for the three major areas brought together in this proposal viz. UWB communication technology, communication over power lines and the power distribution network of a microprocessor.

Chapter 3 discusses the first part of the feasibility study using high frequency modeling of the complete power distribution network in a microprocessor. High frequency models developed at Virginia Tech showed feasibility and also presence of

noticeable pass bands at frequencies beyond 1 GHz. Detailed PDN models available at Intel was studied during an internship and simulations were carried out with existing models. Intel PDN models were valid only up to 200 MHz and high frequency distributed effects were not captured and consequently, the overall response appeared to be that of a low pass filter and no high frequency pass bands were observed. Therefore, a decision was taken to proceed with feasibility study using direct high frequency measurements. Modeling basics were also discussed.

Chapter 4 details the second and more direct feasibility study of the proposal. Measurements were carried out in the 65 nm Pentium 4 processor as well as the 45 nm Core 2 Duo processor. Measurements were carried out in both the cold processor as well as the active processor. Measurements were also carried out in several samples and at different locations, to estimate the process variation from die-to-die as well as the variation of transfer characteristics from one location to the next.

Chapter 5 takes a system level view of the proposed approach. A PDN channel model was developed based on the feasibility study measurements and its impulse response was derived. To complete the channel model, properties and techniques for modeling PDN noise are reviewed. Also, while at Intel, noise measurements were carried out on the PDN of the 65 nm Itanium processor and the 45 nm Core 2 Duo processor. These results are presented in this chapter. The link budget is calculated and the SNR levels at the internal receivers are estimated. The different possible modulation techniques are studied and their trade-offs are presented. BPSK was the modulation scheme of choice. Another important concern viz. the interference caused by the proposed system to the normal operation of the microprocessor is also studied with the help of simulations.

A circuit design approach for transmitting and receiving information modulated with impulses is presented in chapter 7. Challenges in the receiver design are presented and a receiver design was proposed. Different sub-circuits of the receiver are discussed in detail and simulation results of the data recovery block are presented. Later on, challenges in the design of an internal transmitter are studied. A transmitter design is proposed and the different sub circuits are discussed in detail. Finally simulation results of the transmitter are also presented.

## **7.2 Future Work**

There is a plethora of ways in which future work can proceed in this research area. The research area is still very much in the nascent stage and several important questions need to be addressed and answered in a quantifiable manner due to the wide-ranging applicability of this method. The first and foremost is to prove the feasibility of the proposed communication method with a demonstrable implementation. The designs presented in this thesis will be fabricated in Intel process on a future test run. The designs will be tested at Intel as well in the next semesters. The design of the transmitter could be improved for more energy efficient way of driving the PDN. As for the receiver, its sensitivity, offset and reliability are the important concerns.

Another area of further improvement is the system model of the proposed communication system especially the model of the PDN. The model developed at Virginia Tech differed widely from the Intel model primarily because the Intel model failed to capture the high frequency effects. However, since measurement results have been obtained, a more accurate PDN model based on measurements can be developed and used in a system level model. Also, further this model can be used to do a system level study on the communication, modulation techniques, pulse shapes and spreading codes by using BER simulations. The interference level of the proposed communication method to the normal operation of the microprocessor can be determined in a more quantifiable manner.

Along with the feasibility study, several applications can be imagined if ubiquitous access is available to all the internal nodes. Soft errors can be identified and characterized in a smaller time period due to the increased accessibility to the core logic. The so called ‘low-time-constant errors’ resulting from aging and thermal effects can also be monitored using this method and logged for future study. Ubiquitous accessibility to internal core logic with little overhead is a very attractive option in many scenarios and the proposed method could bring about a paradigm shift in the way current and future generation of microprocessors are tested and debugged.

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## Vita

Rajesh Thirugnanam was born in Singampunari, Tamil Nadu, India on Jan 7 1979. He graduated in *first class with distinction* with a Bachelor of Engineering degree in Electrical and Electronics Engineering from College of Engineering, Chennai, Tamil Nadu, India in May 2000.

Later, he graduated with a Master of Science in Electrical Engineering from Ohio State University in June 2003. He worked under Dr. Joanne Degroat at the Mixed Signal Electronic Systems (MISES) Laboratory and studied mixed signal VLSI design. During his M.S. degree, he worked on implementing decimation filters in Field Programmable Gate Arrays (FPGA) for sigma delta modulators. These reconfigurable decimation filters would find application in the software-defined radios.

He moved to the Bradley Department of Electrical and Computer Engineering at Virginia Tech in August 2003 to obtain a Doctorate. He worked under Dr. Dong Ha at the Virginia Tech VLSI for Telecommunications (VTVT) Laboratory as Research Assistant. His current research interests include CMOS implementation of data-converters, GHz range Transconductance-capacitor (Gm-C) filters for ultra wideband (UWB) systems, and power line communications in a microprocessor. He plans to graduate in the Winter of 2008.

He has authored/co-authored several papers in peer reviewed IEEE conferences. He has also applied for a patent disclosure relating to his research. In the summers of 2006 and 2007, he was a graduate research intern at Intel, Santa Clara, CA working on feasibility study of a with a project related to his Ph.D. dissertation and performed high frequency measurements on Intel's 65nm Pentium and the 45nm Core 2 Duo processors. After receiving his doctoral degree, he plans to join Silicon Laboratories in Nashua, New Hampshire.