

Chapter 6

CMOS Class-E Power Amplifier

6.0 Introduction

Last few years have seen an increase in the popularity of the wireless communication systems. As a result, the demand for compact, low-cost, and low power portable transceivers has increased dramatically [Gray and Meyer, 1995]. A proposed solution is single-chip radio transceiver realized in a low-cost CMOS, [Rofougaran, et al, 1998; Cho, et al, 1999]. Compared to other CMOS RF building blocks, CMOS power amplifier receives less amount of research. Since it is known that RF power amplifier consumes most of the power consumption within a transmitter, reducing its consumption power will improve the transceiver performance.

Because of its superior performance over the MOS transistors, Gallium Arsenide (GaAs) transistors have been used extensively to build the RF power amplifiers. GaAs based power Amplifiers have several drawbacks: costly to implement, require high level power supply, and have large size. CMOS power amplifier's performance is limited because of its low breakdown voltage, low current drive, and lossy substrate. In spite of its limitation, sub-micron CMOS prove to be the best process to implement the RF PA.

Recently, RF power amplifiers have been implemented in a low-cost digital CMOS technology. A power-controllable CMOS RF amplifier is presented in [M. Rofougaran, et al, 1994]. The output power can be controlled digitally from a minimum

of 6 μW to a maximum of 20 mW. Su and McFarland report a RF PA, which has been designed and fabricated in a standard 0.8- μm CMOS technology, [Su and McFarland, 1997]. A 1.9 GHz class-E PA is proposed in [Tsai and Gray, 1999]. It employs the mode-locking concept to achieve one-watt output power from 2-V supply at 41% PAD efficiency. Yoo and Huang report a class-E PA, which operates at 900MHz [Yoo and Huang, 2000]. This amplifier can deliver 0.9-watt with 41% power added efficiency to a 50Ω load.

The goal of this chapter is to design a CMOS RF PA with one-watt output power and a high power added efficiency (68%) at 900 MHz. This PA can be used in the European standard for mobile communications (GSM) handset transmitter. Therefore, the proposed amplifier must comply with GSM specifications.

The GSM is considered the most successful digital cellular system. It requires conformance to a strict spectral mask to ensure that the transmitted spectrum does not invade the adjacent spectrum allocation resulting in interference. Non-conforming transmitter signals will degrade the quality of adjacent channels or, in the extreme case, totally jam the neighboring channel. The importance of the Adjacent Channel Power Ratio (ACPR) parameter defines how one particular GSM transmission channel may affect adjacent transmission channels. The bursts sent by the phone have to stay within certain limits that have been defined in the GSM specifications [GSM0505].

6.1 Output Stage

Output stage is the first part need to be designed in the PA circuit. Its function is to deliver the required power to the load. Output stage imposes the upper limits of the PA efficiency and output power. Therefore, designing a good PA start with designing a good output stage. In other words, if the output stage performance fails to meet the specifications, the PA performance will do the same but the opposite is not necessary true.

As mentioned earlier, this PA intended to be used in the GSM system, which uses a constant envelope modulation scheme, Gaussian Minimum Shift Keying (GSMK). A good candidate topology to be used here is the switched-mode output stage.

The CMOS sub micron technology is used to implement the RF circuits, which operates above 800 MHz. With the low breakdown voltage feature, this technology has a power supply limit around 3-V. Tirdad shows that at low voltage mode class-E has higher optimum load than class-B, C, and F [Tirdad, et al, 1995]. This implies that the matching network used for Class-E is simpler and has a lower loss than the one required by the other classes.

The traditional configuration for class-E is the single-ended one shown in fig.6.1. As explained in section 5.1, transistor M1 operates as a switch; M1 is on in a half cycle and off in the other half. The resonance frequency of the output loop has different values when M1 is on and when it is off. This generates harmonic distortion. Fig.6.2 shows the transistor model in both cases, when it is on and off. Resonance frequencies for this typology are given by:

$$\begin{aligned} \omega_o &= 1/\sqrt{L_o \cdot C_o} & M_1 \text{ is } on \\ \omega_1 &= 1/\sqrt{L_o(C_o \cdot C_T)/(C_o + C_T)} & M_1 \text{ is } off \end{aligned}$$

C_T includes C_P and the parasitic capacitance across M_1 .

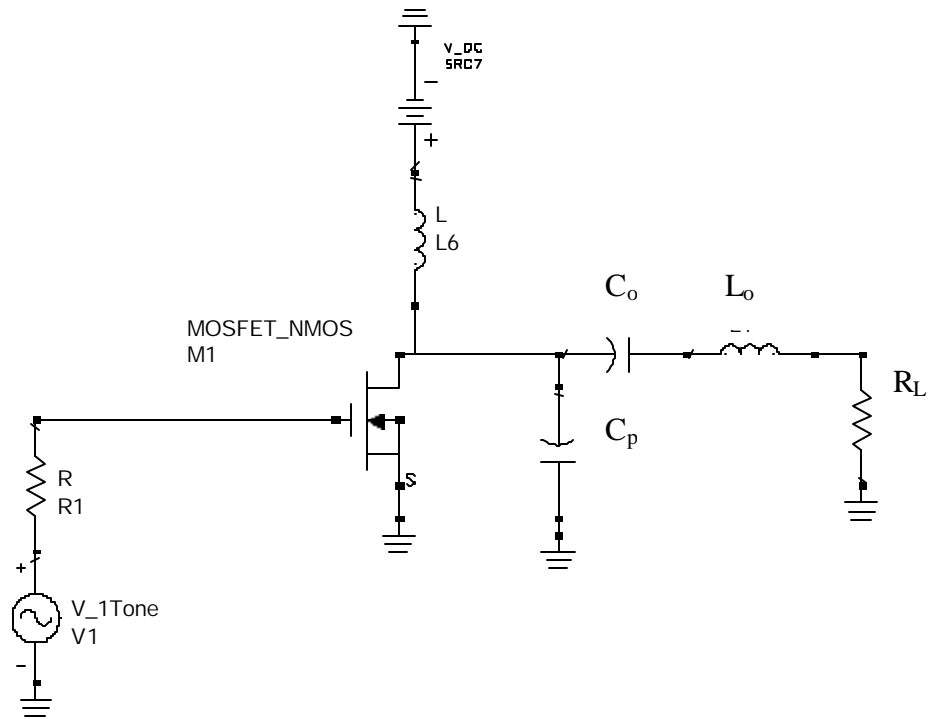


Figure 6.1. Single-ended Power Class-E Amplifier

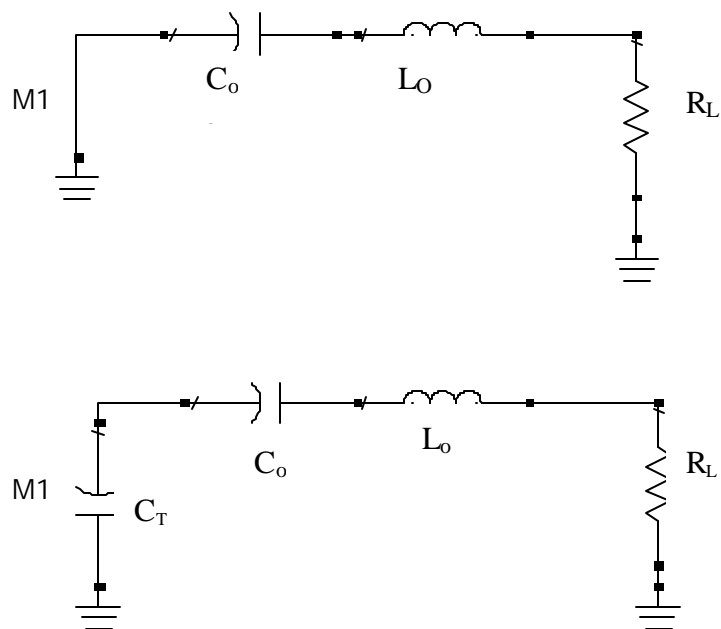


Figure 6.2. Single-ended Class-E equivalent circuit.

Steve and Toumazou proposed a new configuration for class-E, fig.6.3a [Steve and Toumazou, 1999]. As shown in fig.6.3b, the resonance frequencies are as follows:

$$\left. \begin{aligned} w_1 &= 1/\sqrt{L_1 \cdot C_1} \\ w_2 &= 1/\sqrt{L_2(C_2 \cdot C_{T2})/(C_2 + C_{T2})} \end{aligned} \right\} \text{(M}_1 \text{ on and M}_2 \text{ off)}$$

$$\left. \begin{aligned} w_3 &= 1/\sqrt{L_2 \cdot C_2} \\ w_4 &= 1/\sqrt{L_1(C_1 \cdot C_{T1})/(C_1 + C_{T1})} \end{aligned} \right\} \text{(M}_1 \text{ off and M}_2 \text{ on).}$$

Harmonic distortion can be minimized by the proper choice of capacitors and inductors values, $C_1=C_2$ and $L_1=L_2$. In other words, w_1 and w_3 should be equal to the operating frequency w_o . Although this configuration provides a resonance frequency equal to the operating frequency in both cycles, it generates other distortion frequencies, w_2 and w_4 . This can be minimized by maintaining a symmetric typology; C_{T1} should be equal to C_{T2} .

Another disadvantage of fig.6.3 is it uses a PMOS transistor. It is well-known that PMOS transistors have lower transconductance gain and operating frequency compared to the NMOS transistors. Moreover, this typology requires two polarity power supplies.

Mader shows that a maximum frequency of class-E operation for a given device is can be approximated by: $f_{\max} = \frac{I_{\max}}{56.5 \cdot C_T \cdot V_{DD}}$ [T. Mader, 1995]. I_{\max} is the maximum current that the device can provide. Therefore, C_T puts a limit on the maximum operating frequency. Power amplifier requires large transistors to provide the required output power. Thus, the configuration shown fig.6.3a cannot provide good performance at high output power and or high frequency operation.

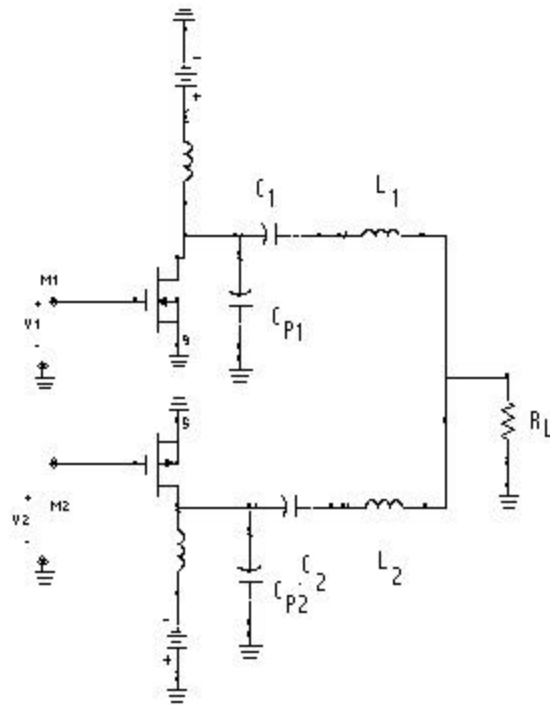


Figure 6.3a. Steve and Toumazou Class-E Amplifier.

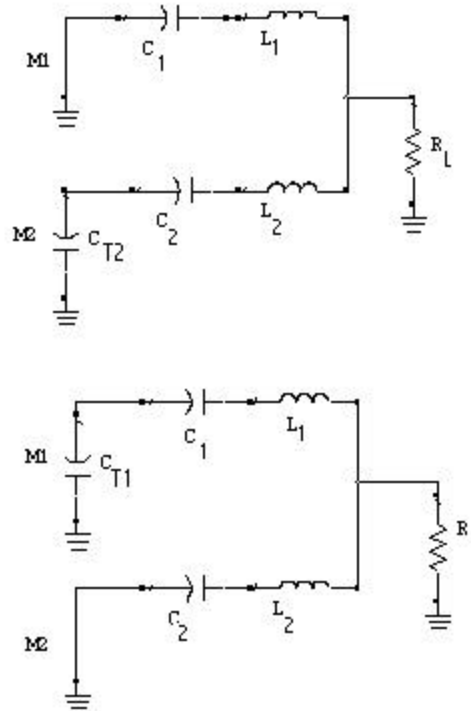


Figure 6.3b. Steve and Toumazou Class-E Amplifier's equivalent circuit.

6.2 Proposed Output Stage

Figure 6.4a shows the proposed class-E output stage. Ideally, M1 and M2 act as switch; one-transistor switches on and the other off alternatively every half cycle. This typology uses NMOS transistors only. The power supply used here is a single polarity one. V1 and V2 have equal amplitude and 180 degrees phase deference. Fig 6.4b shows both cases when one transistor is on and the other is off. By proper selection of C_{p1} and C_{p2} , the resonance frequency will be the same in both cycles,

$\omega_o = 1/\sqrt{L_o(C_o + (C_o \cdot C_T)/(C_o + C_T))}$. In fact, due to the non-linearity of the switches there will be still harmonic distortion. This circuit is expected to generate less harmonics compare to the other circuits.

Figs.6.1, 6.3, and 6.4 were simulated to study their performances. BSIM3 model were used to model the performance of the MOS transistors. The model parameters, HP 0.5 um process, are available in MOSIS' homepage [MOSIS]. Tables 6.1 and 6.2 present a comparison between the performances of the three circuits. The proposed circuit shows better linearity. It has the 3rd and 5th intermodulation components at -32dBc and -34dBc respectively. This shows an improvement of at least 15 dBc and 6 dBc of the 3rd and 5th order intermodulation products respectively over the other typologies. In terms of output power and efficiency, all typologies show a comparable performance at 900 MHz. At 1.9 GHz the proposed circuit shows a better performance due to the lower C_T as explained earlier. Fig.6.5 and table.6.3 present the proposed output stage components' values.

Designing a PA with high efficiency and output power for GSM system is not as difficult as it is for the North American Digital Cellular system (NADC). The reason for that is the former uses a constant envelop modulation, GSMK modulation, and the latter uses a variable envelop modulation, $\pi/4$ QPSK modulation. To meet the NADC specifications, high linearity PAs are used in the transmitter part. Traditionally, these

PAs are class AB or B amplifiers, which operate at a point lower than the compression point. As a result, these PAs have low efficiency and low output power. Among the others alternative techniques, which achieve good linearity, efficiency, and output power is using high efficiency switched amplifier with an additional linearization circuit [Sowlati, et al, 1996; Su and MacFarland, 1998]. Linearization circuits are usually very complex and chip's area consuming.

The better linearity of the proposed output stage over the other configurations open a window for using this configuration in the variable envelope modulation systems. This point can be searched in future work.

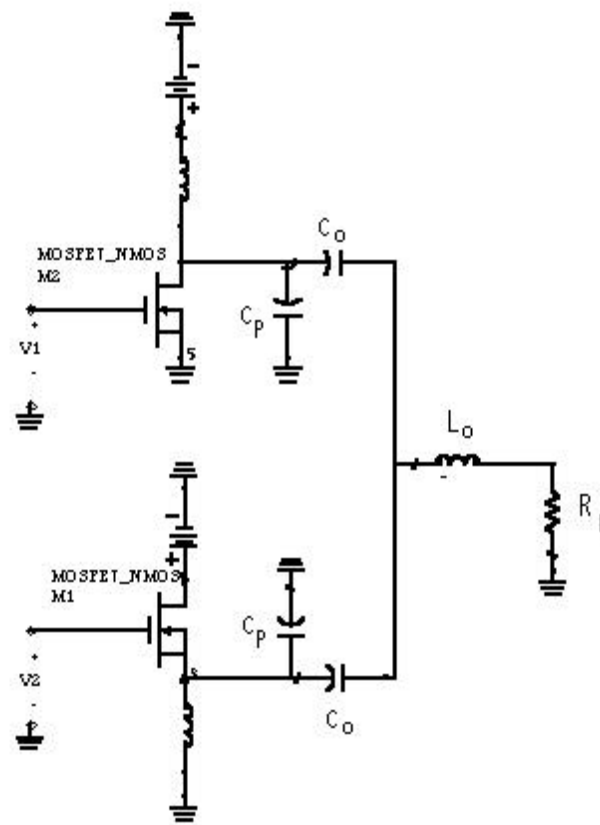


Figure 6.4a. Proposed Class-E Amplifier

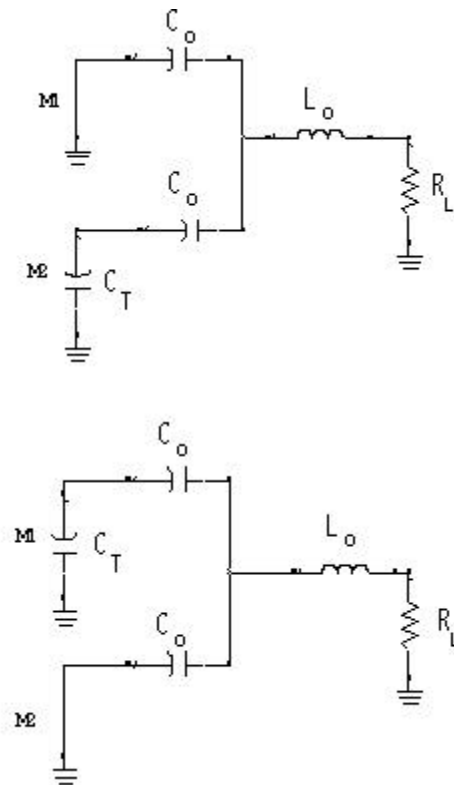


Figure 6.4b. Proposed Class-E Amplifier's equivalent circuit.

TABLE 6.1. Summary of the class-E configurations' performance at 900 MHz.

	Single-Tone Test		Double-Tons test	
	PAD	P _{out} Watt	IM3 dBc	IM5 dBc
Conventional class-E	82%	1.01	-16	-27
Steve and Toumazou	81%	1.08	-17.5	-28
This work	81%	1.05	-32	-34

TABLE 6.2. Summary of the class-E configurations' performance at 1.9 GHz.

	Single-Tone Test	
	PAD	P _{out} (Watt)
Conventional class-E	74%	1.3
Steve and Toumazou	61%	1.3
This work	78%	1.3

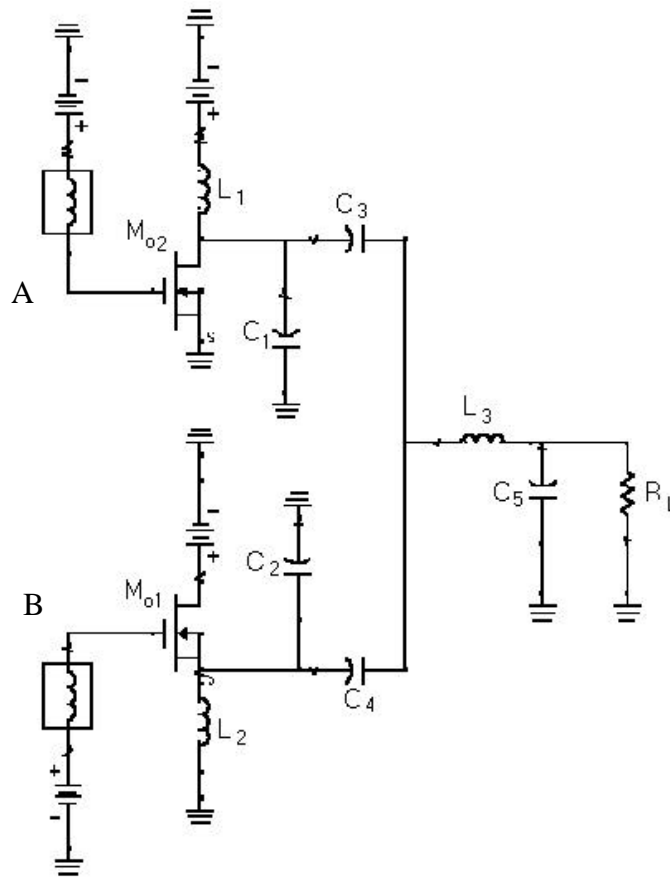


Figure 6.5. The proposed class-E Amplifier's output stage.

TABLE 6.3. The proposed output stage components' values.

Transistor		(W um/L um)	
M _{o1}		10000 / 0.5	
M _{o2}		10000 / 0.5	
Component	Value	Component	Value
C ₁	3.0 pF	L ₁	3.0 nH
C ₂	6.0 pF	L ₂	3.0 nH
C ₃	31 pF	L ₃	3.2 nH
C ₄	15 pF	R _L	50 Ω
C ₅	12 pF		

An important point must be noted here is that with the trends towards the sub micron technology to implement the RF circuits, the breakdown voltage is reduced. This makes the power amplifier design, which requires high peak voltages, difficult task. Yoo and Huang report a power amplifier, which overcomes this limitation [Yoo and Huang, 2000]. This PA employs the class-E configuration with a common-gate switching scheme to achieve one-watt output power at 41% power added efficiency and not to stress the active devices. This approach expected not to give good result at high frequency because of the large total capacitor across the output stage transistor.

Another approach to reduce the peak voltage necessary is to use a differential architecture. In this configuration the peak voltage required at every node in the circuit are reduced by $\sqrt{2}$ compared to the single ended configuration. Another advantage of the differential architecture is the immunity to common-mode noise. Substrate coupling is one of the main noise sources. One drawback of the fully differential configuration is it has a differential output while the antenna is a single ended. Thus a low-cost low-loss balun is required to convert the differential PA output into a single-ended signal without performance degradation.

The proposed output stage, shown in fig.6.4a, is a fully differential configuration where the input voltages are differential and the outputs current are also differential. With this configuration, the need for the balun is eliminated. The reason for this is that the differential current form can be easily switched to a single-ended form by tiding the differential output currents.

6.3 Preamplifier

As mentioned earlier, the power amplifier is designed to deliver one-watt (30dBm) output power at power added efficiency above 60%. The proposed output stage shows a good performance of 82% drain efficiency and one-watt (30dBm) output power. However, to achieve the desired performance, the output stage requires a high peak voltage drive around 4V. The required high voltage drive cannot be delivered by the mixer stage or whatever block might precede the PA.

Thus a high gain preamplifier must be designed to deliver the necessary driver level. A high voltage gain of about 10 mandates a multi stage amplifier. The large size output stage transistor implies the need for the preceding stage to drive a huge capacitor, in this design 20pF. Therefore the first stage of the preamplifier needs to be small to minimize the capacitor seen by the mixer and the final stage of the preamplifier must be large to drive the large capacitor presented by the output stage transistors. In addition, to minimize the capacitive loading an inductor can be used at the gate of the large transistors to resonate its capacitor.

An inductor with moderate value has reasonable impedance at RF frequency. Hence it can be used as the load element instead of the resistor. This will allow the peak voltage to be larger than the voltage supply and in the same time minimize the power dissipation. Since the amplifier intends to be used in a constant envelop modulation, the linearity of the preamplifier is not an issue.

As a summary for the preamplifier specifications, a high voltage gain is needed to drive the output stage transistors to operate as switches. The preamplifier generates the required voltage swing at a node and its 180 degrees phase shifted version at another node. To maintain the overall efficiency close to that of the output stage, the preamplifier DC current need to be small.

Fig.6.6 shows the preamplifier circuit. Input matching network is used to match the preamplifier to a 50Ω source. Capacitors are placed at transistors' drains to resonate with the load inductors. This improves the gain at the desired frequency and reduces harmonic distortion. Table.6.4 presents transistors' ratio and components' values.

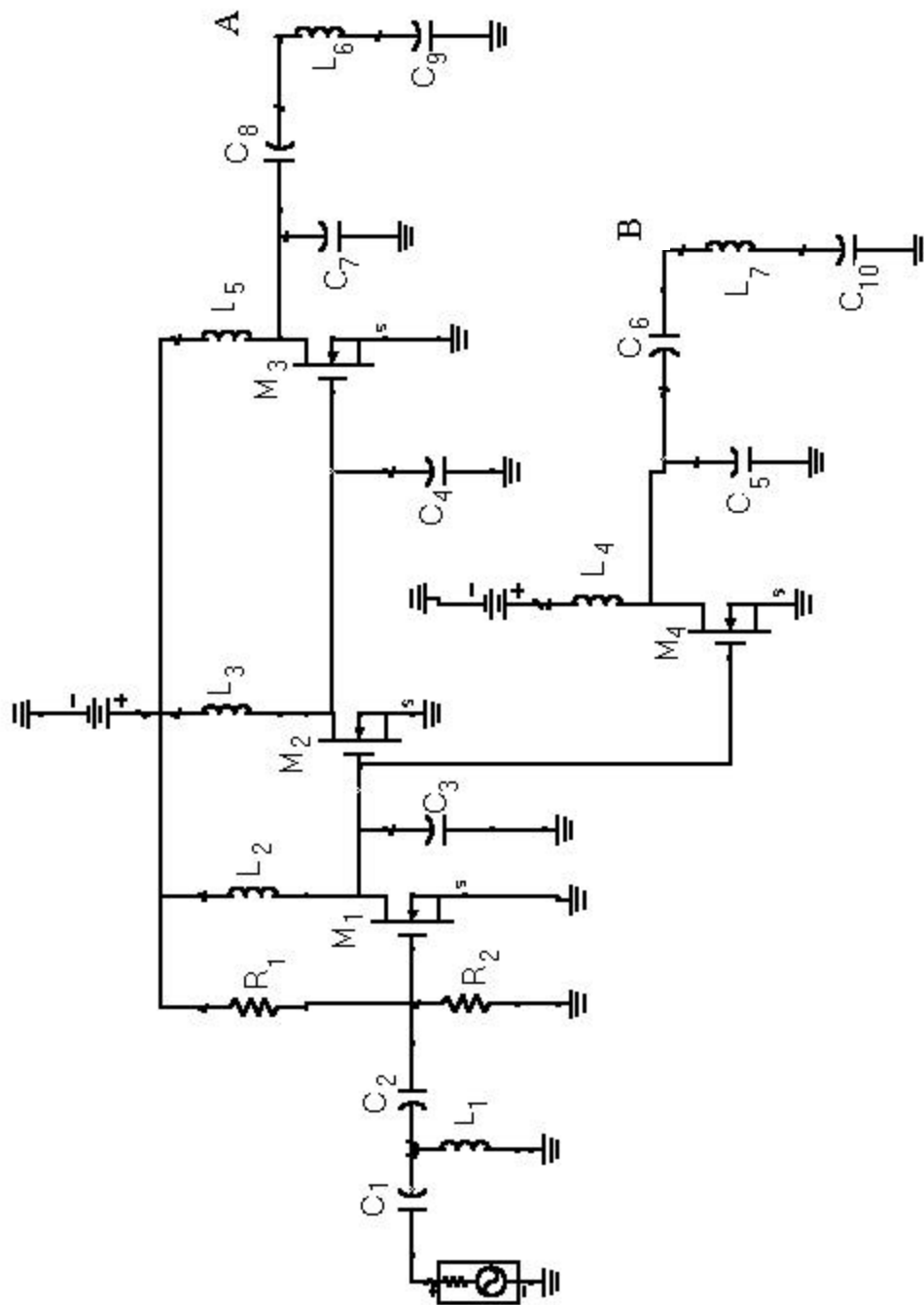


Figure 6.6. The preamplifier circuit.

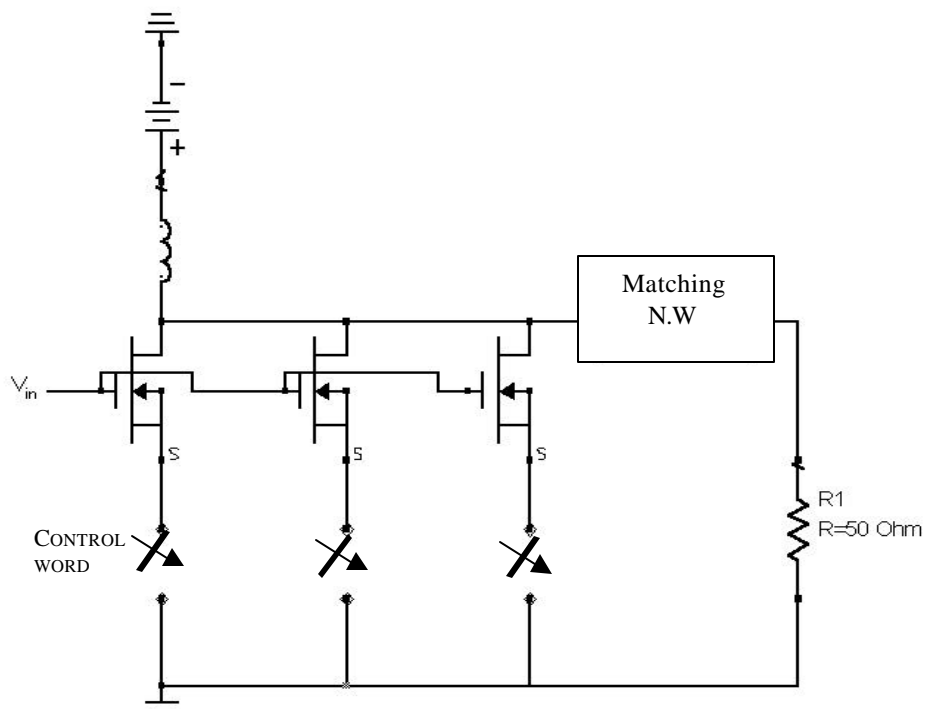
TABLE 6.4. *The preamplifier components' values.*

Component	Value	Component	Value
C ₁	5 pF	L ₁	12 nH
C ₂	15 pF	L ₂	4 nH
C ₃	6 pF	L ₃	4 nH
C ₄	7 pF	L ₄	6 nH
C ₅	8 pF	L ₅	8 nH
C ₆	6 pF	L ₆	3.5 nH
C ₇	8 pF	L ₇	7 nH
C ₈	10 pF	R ₁	350 Ω
C ₉	14 pF	R ₂	350 Ω
C ₁₀	9 pF		
Transistor		(W μm /L μm)	
M1		300 / 0.5	
M2		100 / 0.5	
M3		500 / 0.5	
M4		1000 / 0.5	

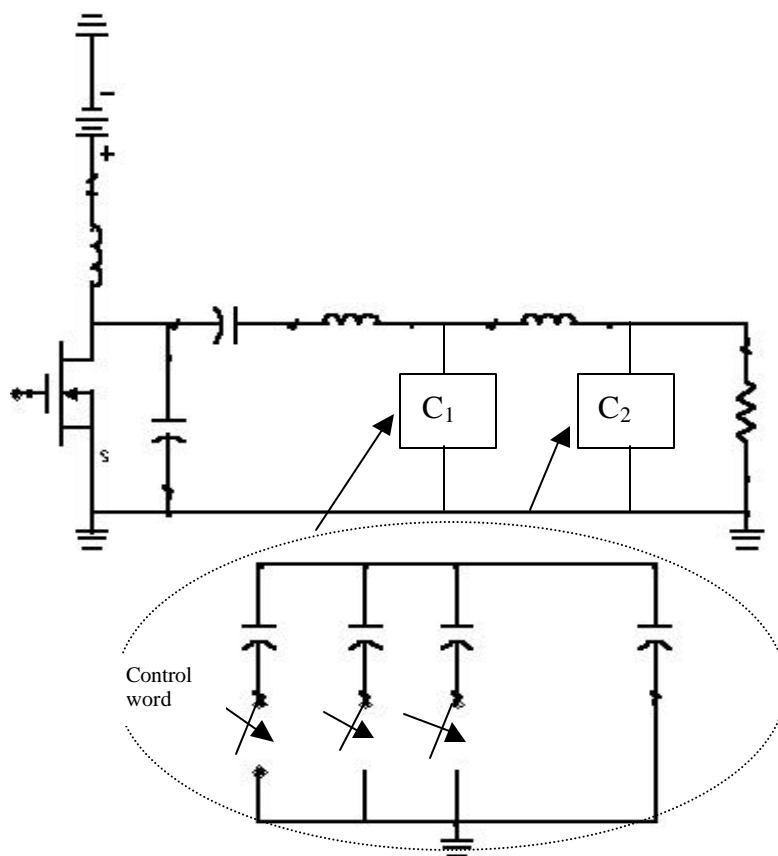
6.4 Power Control Circuit

Power control feature is desirable in modern communication system. With this scheme the power transmission is reduced in the case of low detectable signal is desired and high power transmission when maximum interference rejection is needed. Three techniques have been used to implement controllable power amplifier. In the first technique, the output power is controlled via varying the output-stage driving-signal. This method requires linear output stage with large dynamic range. Another way of controlling output power is by adjusting the DC current of the output stage, which requires an additional complex circuit to control the DC current. In the third one, output stage is consist of an array of NFETs devices with different sizes, which can be switched on and off by applying binary word, fig.6.7a [Rofougaran, et al, 1994]. The common disadvantage of the above techniques is that the maximum efficiency is obtained at the maximum output power and droop sharply if the output power starts to deviate from the peak value.

Recently, Steve and Toumazou present a power controllable class-E amplifier [Steve and Toumazou, 1999]. Tuning the capacitors of the output-matching network controls the output power. As shown in fig.6.7b, control word is used to tune the capacitors. This technique provides a high efficiency over large range of output power values. Although it maintains the high efficiency over smaller range of output power compared to the Steve technique, a simplified version was used in this work. The reason for this is that integrating a high quality factor inductor, which is necessary in the output-matching network, is not yet visible.



a)



b)

Figure 6.7. Power-controllable amplifier
 a) Rofougaran circuit.
 b) Steve circuit.

6.5 Simulation Results

The power amplifier complete circuit consists of the output stage shown in fig.6.5 and the preamplifier shown in fig.6.6. The PA was simulated using the ADS software. BSIM3 model were used to model the performance of the 0.5 um NMOS transistors. The model parameters, HP 0.5 um process, are available in MOSIS' homepage [MOSIS].

The final PA design can deliver 1.05-watt with 68% power added efficiency to a 50Ω load at 900 MHz. The simulated voltage and current waveforms of the PA are shown in fig.6.8. In Fig.6.8a, V_1 and V_2 are the voltage at the drains of M_{o1} and M_{o2} respectively. Fig.6.8b shows the drains currents of M_{o1} and M_{o2} . V_o is the output voltage across the 50Ω load, Fig.6.8c. The power dissipation of the preamplifier and the output stage are 270 mWatt and 240 mWatt respectively. Fig.6.9 and Fig.6.10 depict the output power and efficiency versus the variation of the supply voltage V_{DD} respectively.

To prove its compliance with the GSM specifications, The PA was simulated with a gaussian minimum shift keying (GMSK) modulated input signal. The maximum output power is normalized to compare the performance to the spectrum characteristics mask. The data rate is 270.83 Kbps, and the Gaussian filter bandwidth bit, BT, is 0.3. As shown in fig.6.11, No spectral regrowth is observed.

By adding a capacitor, c_x , to the output stage as shown in fig.6.12, output power is controllable. Fig.6.13 depicts the output power and efficiency versus capacitor c_x values. The output power can be varied from 1.03 Watt to 0.33 Watt with an efficiency of 68% and 25% respectively. Moreover, the droop in the efficiency is not sharp. The main reason for choosing this simple modification, adding c_x , is to maintain the performance of the PA.

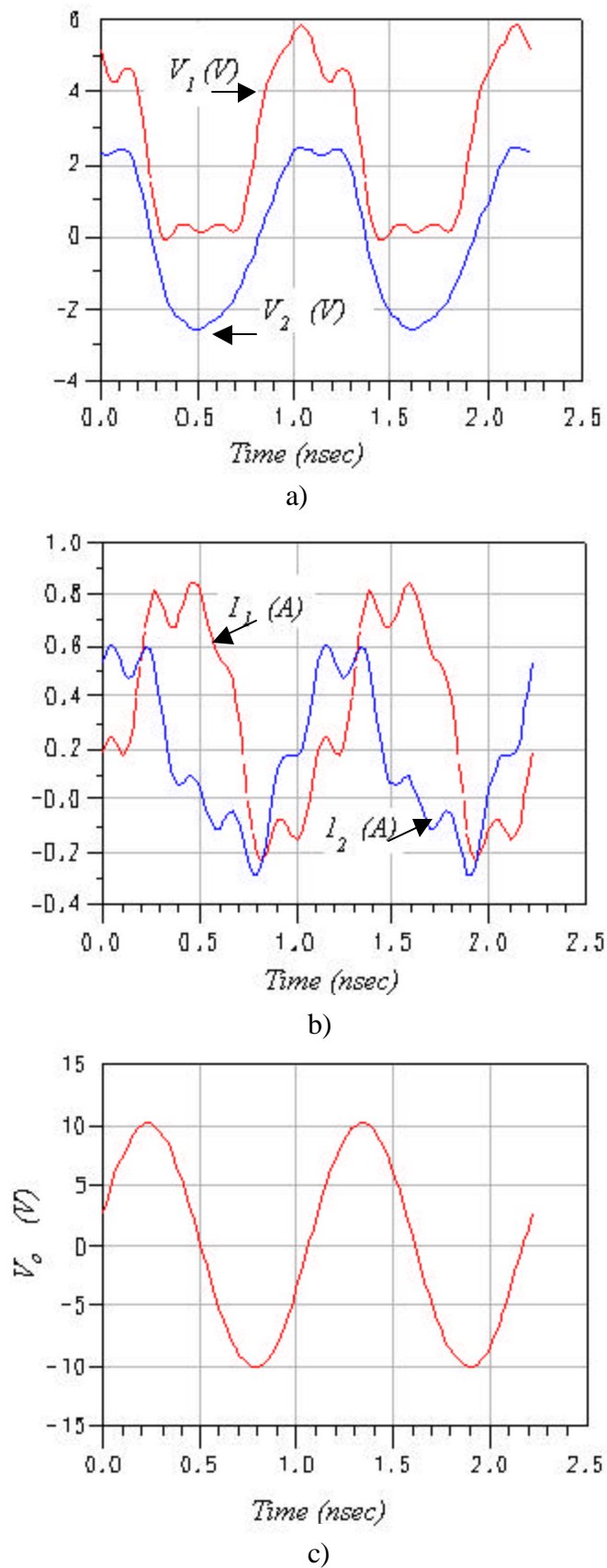


Figure 6.8: a) Drain voltage waveforms.
b) Drain current waveforms.
c) Output voltage waveform.

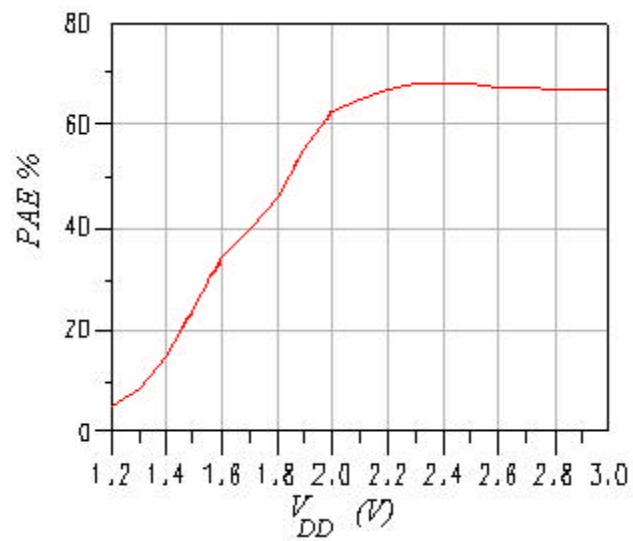


Figure 6.9. Power added efficiency vs. supply voltage.

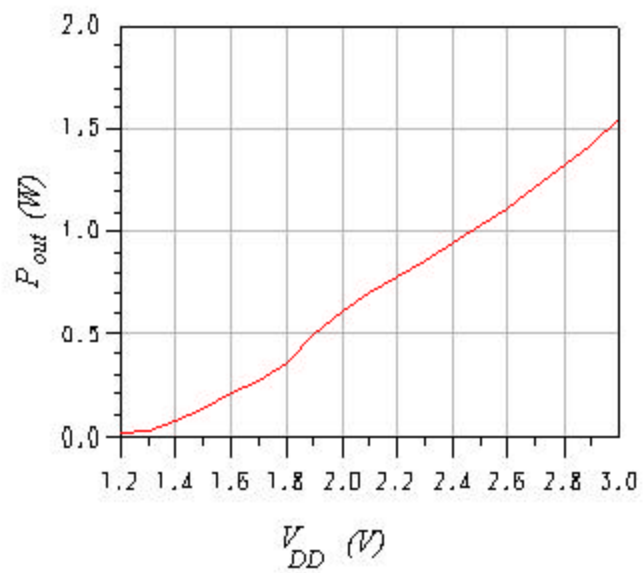


Figure 6.10. Output power vs. supply voltage.

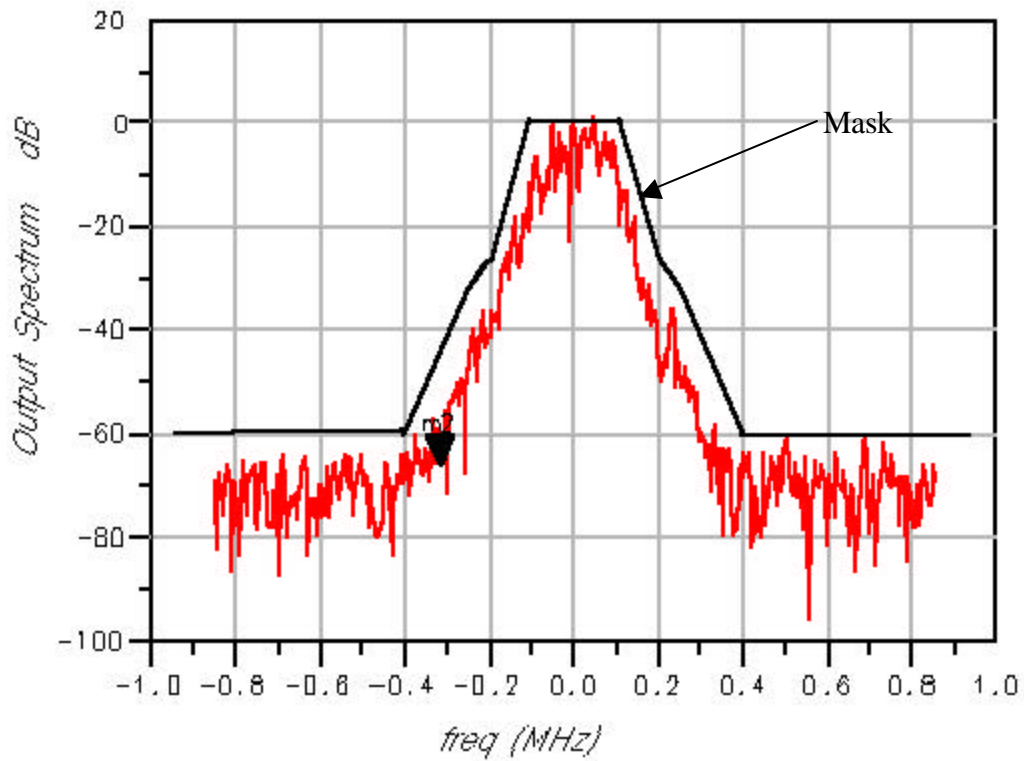


Figure 6.11. PA output spectral and the GSM spectral emission mask.

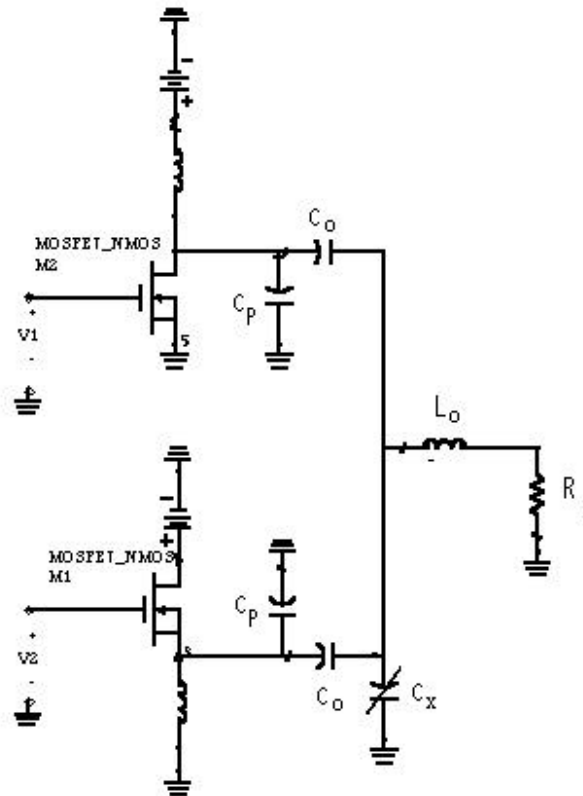


Figure 6.12. The proposed output stage including the variable capacitor c_x .

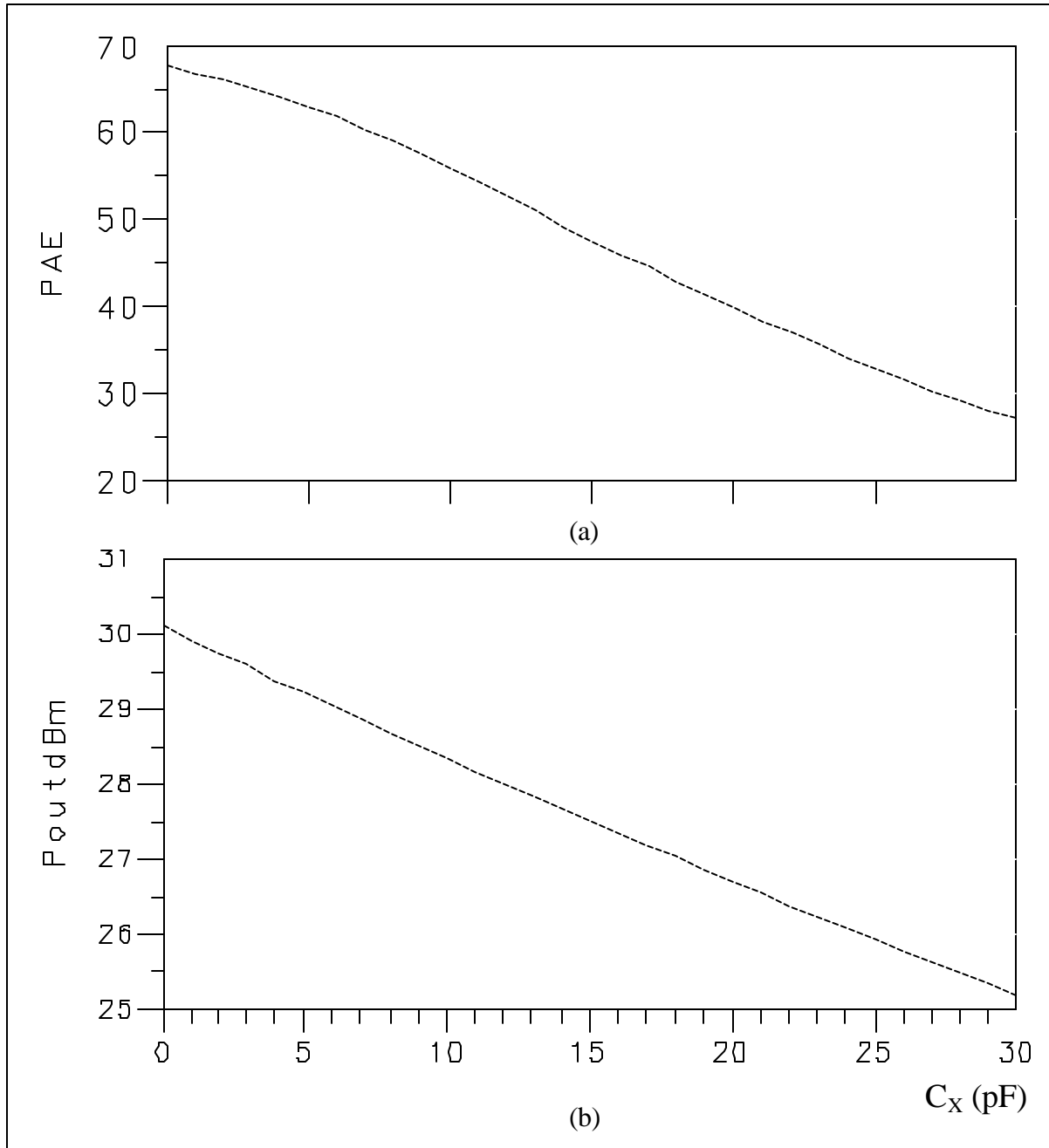


Figure 6.13. a) Power added efficiency vs. capacitor c_x values.

b) Output power vs. capacitor c_x values.

6.6 Layout Issues

Although high conductivity substrate is preferable in digital circuit design to eliminate latch up mechanism and lower substrate noise, high resistivity substrate is recommended for RF circuit to minimize the substrate capacitance. The substrate effect can be modeled as a resistor in series with a capacitor. The resistance under each layer can be calculated using $R = \rho L/A$ formula where ρ is the substrate resistivity, L is the substrate thickness, and A is the layer area. Substrate capacitance is calculated using $C = C_{par} \cdot A$ formula. C_{par} is the capacitance parameter between the desired layer and the substrate and A is the overlap area between the layer and substrate. For simplicity, the substrate model is added at pads only.

Monolithic silicon inductor has poor performance. There are two major reasons for this limitation: the series resistance of the metal and the lossy silicon substrate. The quality factor of the monolithic silicon inductor is around five in the RF range. Although bond-wire inductance is main source for the poor grounding in a circuit, it is used extensively to build inductors with high performance. All the inductors used in this work but the one used in the matching networks are bond-wire inductors.

Integrated capacitor has associate parasite capacitance. The parasitic capacitance can be modeled by adding 10% of the main capacitor at one of its terminal.

In order for an integrated circuit to be useful, it must have physical connections to the outside world. Packaging circuits operate at frequency greater than 800 MHz is difficult task. There are two major problems: circuit grounding and dielectric effects. Large ground-inductance and thermal-resistance affect circuit's reliability and performance. To date all the published MOS PA performance were measured from the die directly.

The layout practical issues mentioned above except the packaging one have been taken into account in the design. As a result, the performance reported earlier degrades slightly. The PA performances including the above practical issues are as follows: output power of 1.05 watt and power added efficiency of 60% at 900 MHz. To the best of our knowledge, this performance is better than the published ones.