

## Chapter 7

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### Stress Effect of ILD

A study on the stress effect of ILD silicon oxide layer is described in this chapter. This section was published in Applied Physics Letters Vol. 74, No 16, p.2286, April 1999 under the title “*Deposition-Temperature-Dependent Stress of Capping Oxide and its Effect on Pt/Pb(Zr<sub>1-x</sub>Ti<sub>x</sub>)O<sub>3</sub>/Pt Ferroelectric Capacitor*”. The authors are Bon Jae Koo, Yoon jong Song, Sung Yung Lee, Dong Jin Jung, Byung Hee Kim, Kinam Kim, Youngsoo Park , and June Key Lee

#### ABSTRACT

Two different interlayer dielectric (ILD) materials, Electron Cyclotron Resonance Chemical Vapor Deposition Oxide (ECR-OXIDE) and Plasma Enhanced Chemical Vapor Deposition TEOS Oxide (PE-TEOS), were prepared at 400 °C and 200 °C, respectively, on silicon substrates and Pt/Pb(Zr<sub>1-x</sub>Ti<sub>x</sub>)O<sub>3</sub> (PZT)/Pt capacitors. It was found that the ILD deposition temperature is a most important parameter for minimizing the degradation of remnant polarization ( $P_r$ ) during the ILD deposition. Since the stress of PZT capacitor strongly depends on the ILD deposition temperature, the PZT capacitor with PE-TEOS showed more compressive stress than that with ECR-OXIDE, which results in severe  $P_r$  degradation of PZT capacitor with PE-TEOS. This large stress effect of PE-TEOS was confirmed by X-ray diffraction (XRD) patterns in which the d-spacing of (111) PZT films with PE-TEOS was much larger than that of PZT films with ECR-OXIDE. Therefore, the low ILD deposition temperature is a key parameter for achieving an ILD integration without any  $P_r$  degradation.

## §1. INTRODUCTION

Ferroelectric Random Access Memory (FRAM) has been considered as a future memory device due to its nonvolatility, high speed, and low voltage operation. In particular,  $\text{Pb}(\text{Zr}_{1-x}\text{Ti}_x)\text{O}_3$  (PZT) has been attracted as a promising capacitor material for FRAM device application because of its excellent ferroelectric properties [1,2]. In order to achieve high density and logic embedded FRAM devices, Inter-Layer Dielectric (ILD) materials should be prepared on ferroelectric capacitor without any degradation of ferroelectric properties. Typically,  $\text{SiO}_2$  films prepared by Chemical Vapor Deposition (CVD) or plasma technique have been used as ILD materials, and their processing damages such as  $\text{H}_2$  attack and plasma damage have been evaluated [3-5]. In particular, the stress generated by depositing the oxide layer is considered as one of vital factors in degrading the ferroelectric properties [6-8]. However, the ILD stress effect on the ferroelectric capacitors has not been systematically investigated. In this paper, Electron Cyclotron Resonance Chemical Vapor Deposition Oxide (ECR-OXIDE) and Plasma Enhanced Chemical Vapor Deposition TEOS Oxide (PE-TEOS) are used as ILD materials for Pt/PZT/Pt capacitor, and a key processing parameter for minimizing the undesirable stress effect was investigated.

## §2. EXPERIMENTAL PROCEDURE

The stress effect by capping ILD films was evaluated as follows. First, ECR-OXIDE and PE-TEOS were prepared at 200 °C and 400 °C, respectively, on silicon substrates, and their stress characteristics were measured from 25 to 450 °C using TENCOR stress measurement system. The thickness of deposited oxide layer was about 450 nm. Second, the capacitor stacks were formed on silicon substrate to estimate stress characteristics of the capacitor stacks. The capacitor stacks were fabricated as following sequence.  $\text{TiO}_2$  adhesion layer (50nm) and bottom Pt (270nm) were deposited on the  $\text{SiO}_2$ /silicon substrate and then PZT (250nm) was coated by sol-gel process on the Pt/ $\text{TiO}_2$

and crystallized at 650 °C in O<sub>2</sub> ambient for 30 minutes. The top Pt (200nm) and the barrier TiO<sub>2</sub> (100nm) were sputtered on PZT film. After the barrier TiO<sub>2</sub> (100nm) was sputtered, the stress was measured from 25 to 450 °C. After the evaluation of the stress of the capacitor stacks, ILD oxide (1,000nm) was deposited on the capacitor stacks using ECR-OXIDE or PE-TEOS and the stress characteristics were evaluated again with the same method. In order to investigate the stress effect of the ILD layer on PZT films, the d-spacing of PZT (111) plane was calculated by X-ray Diffraction (XRD) patterns before and after ILD deposition. To evaluate electrical properties of ferroelectric capacitors, the patterned capacitors with different capping oxides were contact etched and connected to metal line. The ferroelectric properties were measured by RT6000SI system.

### §3. RESULTS AND DISCUSSION

Figure 7-1 shows the hysteresis loops of Pt/PZT/Pt capacitors covered with ECR-OXIDE and PE-TEOS at 200 °C and 400 °C, respectively. The PZT capacitors integrated by PE-TEOS exhibited severe remnant polarization ( $P_r$ ) degradation, while the PZT capacitors by ECR-OXIDE maintained their ferroelectric properties. Since both PE-TEOS and ECR-OXIDE have similar H<sub>2</sub> and plasma damage, the severe  $P_r$  degradation was considered mainly due to the stress effect of the PE-TEOS layers. Therefore, in order to investigate how to minimize the undesirable stress effect of ILD processing on ferroelectric properties, the stress characteristics of the oxide layers were examined. Figure 7-2 shows thermal stress curves of ILD films on silicon substrates. It was observed that ECR-OXIDE was more compressive and had better thermal stability than PE-TEOS. This implies that ECR-OXIDE is denser and has larger intrinsic stress than PE-TEOS. However, when the ILD films were prepared on the PZT capacitor stacks, the deposited oxides showed totally different stress behavior. Figure 7-3 shows the stress characteristics of two different oxide layers on the PZT capacitor stacks. Unlike on silicon substrates, PE-TEOS on the PZT capacitors exhibited more compressive stress than ECR-OXIDE. Especially, the initial

stress value of PE-TEOS at room temperature was  $-2 \text{ Gdyne/cm}^2$ , which indicates that PE-TEOS on PZT capacitors generates large compressive stress and eventually degrades the ferroelectric properties. These different initial stress values might be attributed to the stress dependence of PZT capacitors on the temperature before depositing ILD layers. Figure 7-4 shows the stress characteristics of Pt/PZT/Pt capacitor stack before ILD deposition. It was observed that the stress appreciably changed from tensile to compressive as a function of temperature. It means that the stress of PZT capacitor itself is very sensitive to the temperature, and thus the ILD deposition temperature is very crucial factor in determining the final stress values of the PZT capacitor stacks after depositing the ILD layer. When ECR-OXIDE was deposited at  $200 \text{ }^\circ\text{C}$  on PZT capacitor stacks, the capacitors had tensile stress of  $5 \text{ Gdyne/cm}^2$ , which results in small stress change of PZT capacitor before and after the ILD oxide deposition. However, as PE-TEOS was prepared on the PZT capacitors at a deposition temperature of  $400 \text{ }^\circ\text{C}$ , the capacitors were under large compressive stress of  $16 \text{ Gdyne/cm}^2$  because the stress was severely dependent upon the ILD deposition temperature. Therefore, the PZT capacitor stacks capped with PE-TEOS possess relatively larger stress than that with ECR-OXIDE, which finally degraded the ferroelectric properties. This large stress effect of PE-TEOS on the PZT capacitor was confirmed by using X-ray diffraction patterns in which the d-spacing of (111) PZT plane in the capacitors was shown. Figure 7-5 shows the measured d-spacing values of (111) oriented PZT crystal. It was found that the d-spacing of (111) PZT plane in Pt/PZT/Pt capacitor capped with PE-TEOS was larger than that of PZT in Pt/PZT/Pt capacitor with ECR-OXIDE. The large d-spacing in the PZT capacitor with PE-TEOS might be attributed to the stress effect of the oxide layer on the PZT films. These results indicate that the oxide deposition temperature is a critical processing parameter for minimizing the ILD deposition stress effect. Therefore, the  $P_r$  degradation of PZT capacitors with the PE-TEOS layers can be minimized by reducing the deposition temperature of the oxide layers from  $400$  to  $200 \text{ }^\circ\text{C}$ . Figure 7-6 shows that the hysteresis loops of Pt/PZT/Pt capacitor capped with PE-TEOS films deposited at  $400 \text{ }^\circ\text{C}$  and  $200 \text{ }^\circ\text{C}$ , respectively. The hysteresis loop of PZT capacitor was degraded by depositing the

PE-TEOS at 400 °C, while the PZT capacitor capped with the oxide layer deposited at an low temperature of 200 °C did not exhibit any appreciable  $P_r$  degradation.

#### §4. CONCLUSION

In conclusion, it was found that the  $P_r$  degradation during ILD processing was closely related with the ILD deposition temperature, which plays a dominant role in determining the stress of PZT capacitor. Therefore, in order to minimize the undesirable stress effect of ILD materials and achieve robust ILD integration, it is desirable to prepare the ILD layers at a low deposition temperature.

#### §5. REFERENCES

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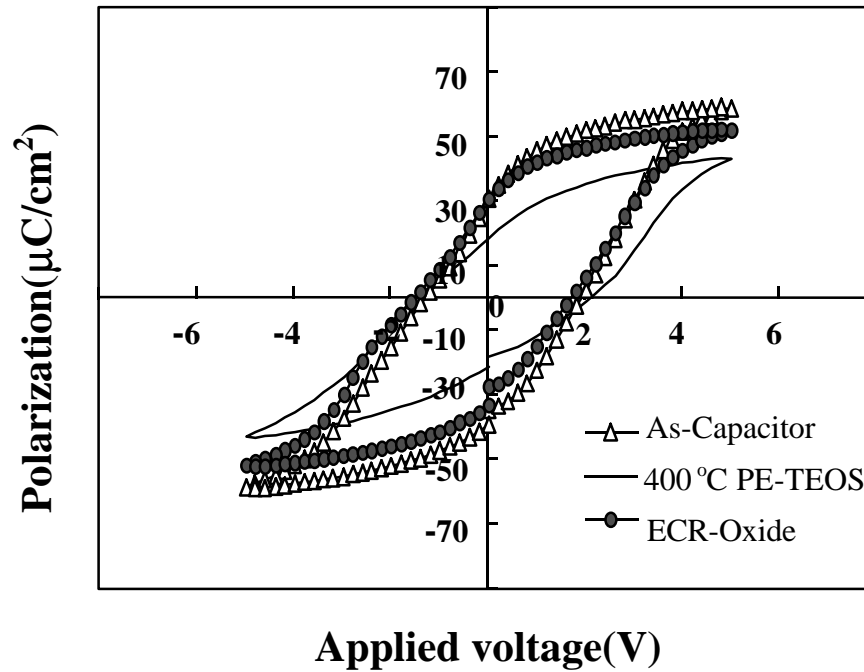


Figure 7-1. The hysteresis curves of Pt/PZT/Pt capacitors covered with ECR-OXIDE and 400 °C PE-TEOS.

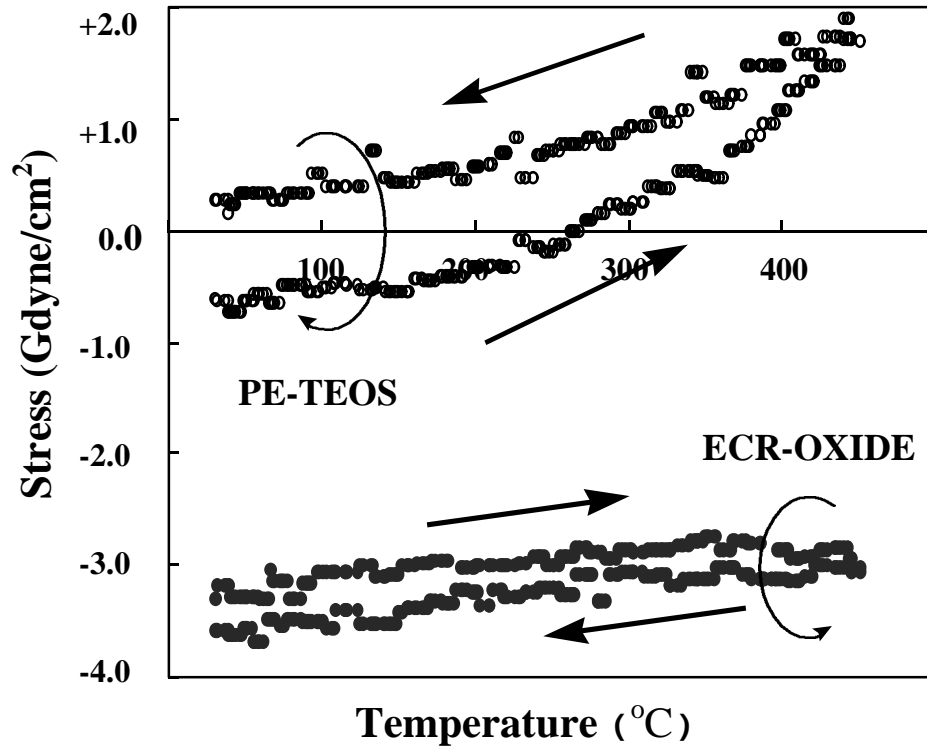


Figure 7-2. The stress characteristics of ECR-OXIDE and PE-TEOS on Silicon

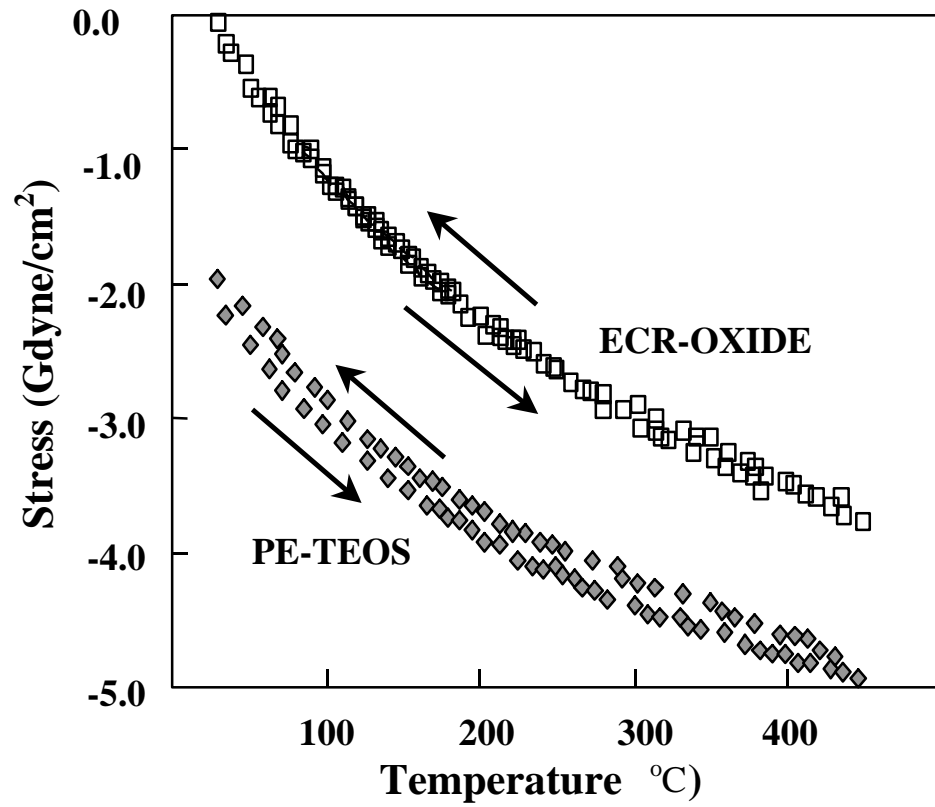


Figure 7-3. The stress characteristics of ECR-OXIDE and PE-TEOS on the capacitor stack. Tensile stress from PE-TEOS deposition.

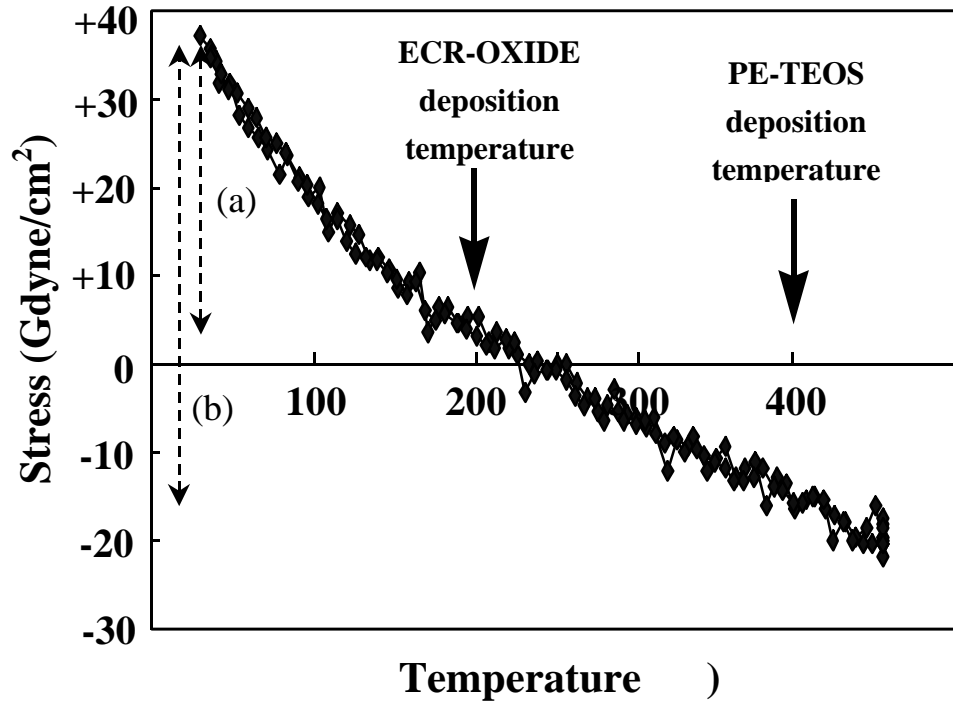


Figure 7-4. The stress characteristics of the capacitor stack and the deposition temperature of ECR-OXIDE and PE-TEOS. (a) Tensile stress at ECR-OXIDE deposition temperature (b) Compressive stress at PE-TEOS deposition temperature.

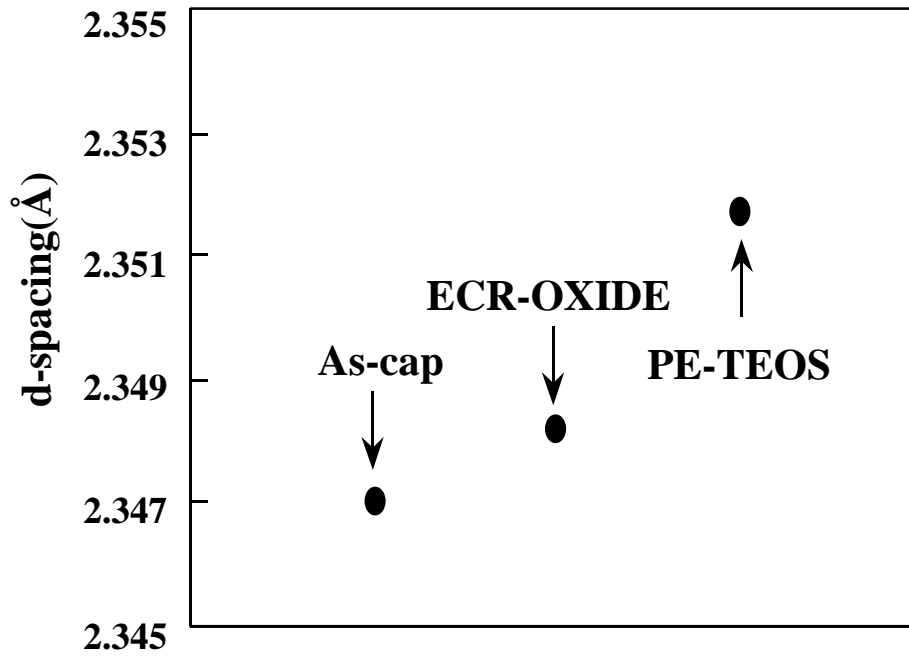


Figure 7-5. The measured d-spacing variation of PZT (111) plane before and after ECR-OXIDE and PE-TEOS.

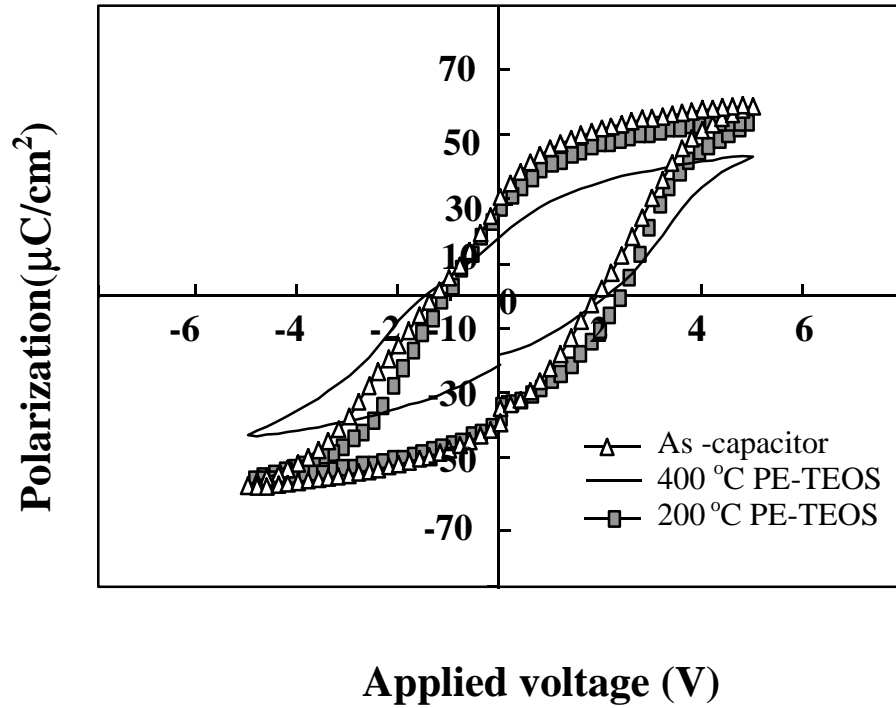


Figure 7-6. The hysteresis curves of Pt/PZT/Pt capacitors covered with 200 °C and 400 °C PE-TEOS.

## VITA

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June Key Lee was born and raised in South Korea. He received his BS and MS degrees in Chemistry Department in 1992 from Korea Advanced Institute of Science & Technology. He then started his doctoral research in the department of Materials Engineering Science at Virginia Polytechnic Institute and State University under supervision of Dr. Seshu B. Desu. Most of his work is related with process issues of perovskite ferroelectric memory devices. Currently he is working in Samsung Advanced Institute of Technology.